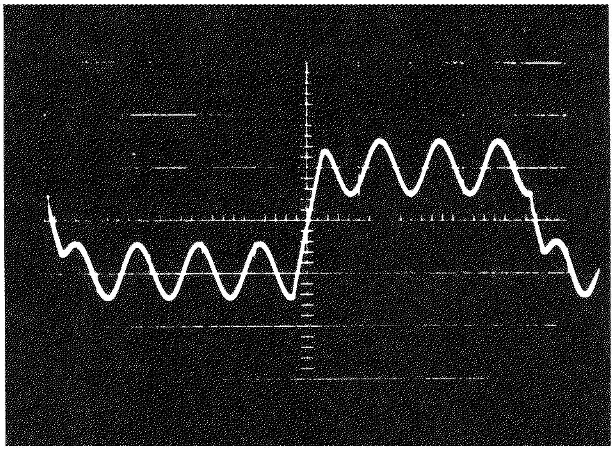
An Overview Of SID and TIM

Walter G. Jung, Mark L. Stephens, and Craig C. Todd

Part III — Analysis and Design of Amplifiers for Minimum SID

Calculation of Slew Induced Distortion



Thus far, little has been said in the literature about how to calculate slew induced or transient intermodulation distortion. This is, no doubt, due to the complexity of the problem, especially handling the frequency dependence of the amplifier stages and the incorporation of feedback. There is, however, a straightforward technique that can be used to find closed-form expressions for every possible harmonic or intermodulation distortion component. The technique involves forming a Volterra series to characterize the output as a function of some input variable [57]. The coefficients of the Volterra series can then be used to find the magnitude and phase of all distortion products. This technique has been widely used to predict distortion in radio frequency circuits with a high degree of accuracy.

Unfortunately, it takes more time and space to explain the technique itself than it does its application to a given problem. For this reason, we have not included a full analysis within the article and direct the interested reader to the reference cited. However, with appropriate assumptions and simplifications, many useful features of the Volterra series technique can be used to find approximate expressions for SID. These are conceptually easier to understand and are quite accurate for relatively small distortion conditions.

Consider a 741-type operational amplifier, which can be broken down into two basic stages, an input transconductance amplifier and an integrating amplifier. These are shown in Fig. 27. The transconductance stage is assumed to be the dominant nonlinearity and consists of a symmetrical saturating-type characteristic which is independent of frequency. The nonlinear characteristic (formed by a double differential pair) is modeled as a current source output Δi, for an input differential voltage ΔV, and can be represented by

$$\Delta i = I_K \tanh \left[\frac{\Delta V}{4V_T}\right] \qquad (21)$$

where $V_T = KT/q$ or approximately 26 mV at 300° K and I_K = the bias current of the stage. The graph of equation (21) is shown in Fig. 28.

Equation 21 and Fig. 28 differ from equation 13 and Fig. 6b in our previous example of Part I, because the 741 input stage has a *pair* of transistors on each side. Equation (21) in its present form will not allow closed-form expressions for distortion. It must be expressed as a truncated power series with variable ΔV to complete the calculations, and this is shown in equation (22).

$$\tanh x = x - \frac{x^3}{3} + \ldots + \ldots \qquad (22)$$

Thus combining (21) and (22) we have

$$\Delta i = I_k \tanh \left[\frac{\Delta V}{4V_T}\right] \cong I_K \left[\left(\frac{\Delta V}{4V_T}\right) - \left(\frac{\Delta V}{4V_T}\right)^3 \frac{1}{3} + \ldots\right]. \qquad (23)$$

The first term in the power series is the desired linear component, and the cubic term (and other higher order terms) form undesirable distortion products. Distortion will eventually be calculated from (23) after making some additional necessary assumptions.

The second stage in the 741, the integrator, is assumed to be ideal and has a gain characteristic G(f) which is proportional to 1/f. This is expressed by

$$G(f) = K_2/f. \qquad (24)$$

There is a $\pi/2$ phase shift in (24) which has been neglected. The reason for this will become evident as the calculation progresses.

The constant K_2 is determined by the overall gain of the composite amplifier, which must be approximately unity at a frequency of 1 MHz to make our circuit model represent the performance of a real 741-type op amp.

The actual gain characteristic of a 741 op amp is summarized by the Bode plot in Fig. 29. For most audio-frequency calculations, it is convenient to neglect the low frequency pole at 10 Hz and to assume infinite d.c. gain and a constant, gain-bandwidth product. This has a negligible effect on calculations, since it will be shown that the distortion is determined by the available loop gain at high frequencies.

The open loop gain for this approximation is specified by

$$\text{open loop gain} = \frac{V_{out}}{\Delta V} = \frac{10^6}{f}. \qquad (25)$$

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By combining equations (23), (24) and (25), the constant K_2 can be expressed in more familiar terms. At a frequency of 1 MHz we have:

$$Vout/\Delta V = 1 = \left[\begin{array}{l}\text{gain of} \\ \text{transconductance} \\ \text{stage}\end{array}\right] \left[\begin{array}{l}\text{gain of} \\ \text{integrator}\end{array}\right]$$

$$1 = \frac{I_k}{4V_T}\left[\frac{K_2}{10^6}\right] \qquad (26)$$

$$K_2 = \frac{4V_T}{I_K} \times 10^6. \qquad (27)$$

$$\text{And thus } G(f) = \frac{4V_T \times 10^6}{I_K} \times \frac{1}{f}. \qquad (28)$$

The 741-type op amp that has been developed thus far is now placed in an inverting gain configuration with resistive feedback components. The feedback network is assumed to be linear and independent of frequency. The circuit used for distortion calculations is modeled in Fig. 30. In this circuit, a feedback factor ß can be specified as a function of R_1 and R_2

$$ß = R_1/(R_1+R_2). \qquad (29)$$

Since the closed loop gain G is equal to R_2/R_1, we have

$$ß = \frac{R_1}{(R_1+R_2)} = \frac{1}{(1+|G|)}. \qquad (30)$$

For inverting gains of 1, 10, and 100 the factor ß is 1/2, 1/11 and 1/101, respectively.

Additional assumptions that must be made to simplify calculations are:

1) Small distortion conditions exist (<1%). This enables a power series expansion of the transconductance nonlinearity.

2) The distortion consists of only odd-order products because of symmetry, and, because of 1), the distortion is dominated by third-order terms.

3) The distortion is reduced by the magnitude of the factor (1 + loop gain), at the frequency of the distortion product. It is further assumed that loop gain is much greater than 1, so that distortion is reduced by approximately the magnitude of the loop gain. Any phase shift in the loop gain can therefore be neglected.

A harmonic distortion analysis will be developed here to compare with measured data, although an intermodulation analysis could also have been pursued. The final result will solve for harmonic distortion (which is dominated by the third harmonic) as a function of output voltage level, frequency, and feedback factor (or closed loop gain).

The following method will be used to solve for harmonic distortion. First, an output level V_o and frequency f will be specified. Then using (25), ΔV will be calculated and used in (23) to find open-loop distortion. Finally the loop gain will be computed and used to predict the closed-loop distortion.

For a sinusoidal output voltage of $V_o \cos 2\pi ft$, we can compute ΔV from (25)

$$\Delta V = \frac{[Vo \cos(2\pi f)t]}{(10^6/f)} \qquad (31)$$

If this ΔV is substituted into (23) and simplified, the resulting equation will show an open-loop distortion ratio of:

$$\frac{\text{magnitude of 3rd harmonic}}{\text{magnitude of fundamental}} = \frac{\left(\frac{\Delta V}{4V_T}\right)^2}{12} =$$

$$\begin{array}{l}\text{Distortion} \\ \text{(open loop)}\end{array} = 1/12 \left(\frac{Vo\, f}{4V_T \times 10^6}\right)^2 \qquad (32)$$

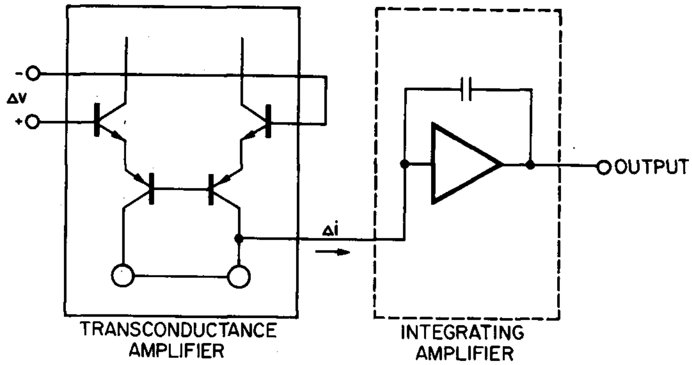


Fig. 27 — Two-stage model of an op amp.

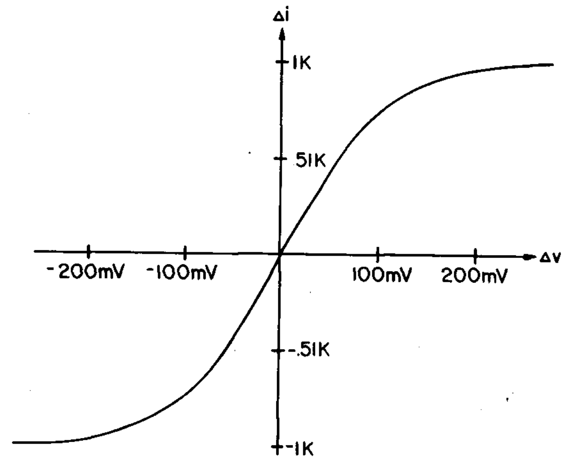


Fig. 28 — Transfer characteristics of a transconductance amplifier.

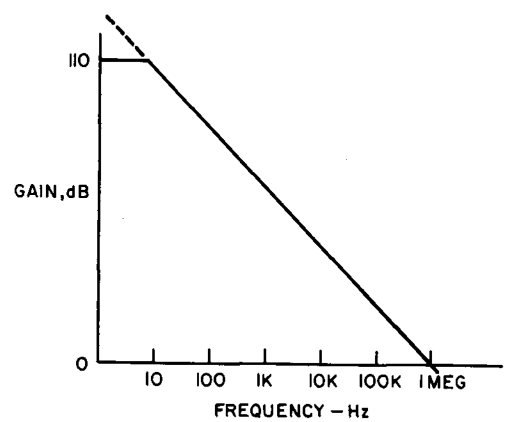


Fig. 29 — Gain-frequency characteristics for a 741 op amp.

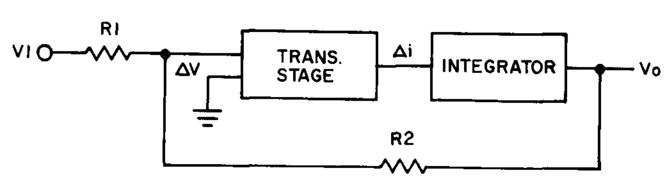


Fig. 30 — Model amplifier with feedback applied.

The open-loop distortion is reduced by the loop gain at the third harmonic frequency, 3f, and by the integrator frequency response which attenuates the third harmonic by a factor of 3. The loop gain at frequency 3f is

$$\text{loop gain} = \left(\frac{I_K}{4V_T}\right) \times \left(\frac{4V_T \times 10^6}{I_K\, 3f}\right) \times ß = \frac{10^6}{3f} ß. \qquad (33)$$

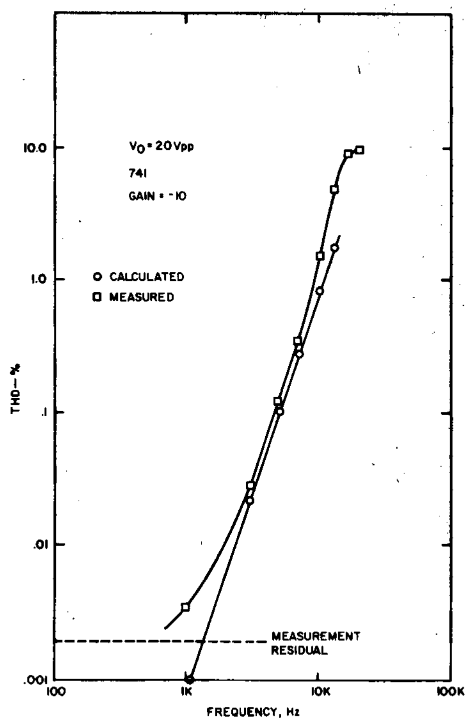


Fig. 31 — Calculated and measured distortion vs. frequency for a 741 at a gain of -1.

Therefore the closed loop distortion is

$$\frac{\text{distortion}}{\text{(closed loop)}} = \frac{\text{distortion (open loop)}}{\text{loop gain}} =$$

$$= \frac{1}{3}\left[\frac{\frac{1}{12}\left(\frac{V_o f}{4V_T \times 10^6}\right)^2}{\left(\frac{10^6 ß}{3f}\right)}\right] \qquad (34)$$

$$\text{THD(3rd)} = \frac{V_o^2 f^3}{12(4V_T)^2 ß \times 10^{18}} = \frac{V_o^2 f^3}{1.29 \times 10^{17} ß}. \qquad (35)$$

Equation (35) shows that harmonic distortion should vary directly with the cube of the input frequency, directly with the square of output voltage, and inversely with the feedback factor, ß. In order to test the accuracy of this equation, calculated data for distortion was compared directly with measured THD data from a 741 amplifier. Figures 31, 32 and 33 compare calculated and measured distortion for a constant-amplitude, swept-frequency test condition for three values of feedback factor, ß. Figure 34 compares calculated and measured distortion for a constant-frequency, swept-amplitude test condition, also for three values of feedback factor. The agreement is generally good and is excellent for the swept frequency tests. At lower distortion levels, the agreement deteriorates due to the noise floor of the distortion analyzer.

At higher distortion levels, the agreement deteriorates due to large distortion conditions, that is, the fundamental assumptions in developing the calculation are violated. The anomalous behavior of the G = 100 test results is due to the loop gain falling below unity at 10 kHz, which also violates a basic assumption of the calculation. Figure 34 indicates an additional crossover type of distortion that dominates at low signal levels and masks the true distortion characteristics. It should be clear from all the figures that increasing feedback *reduces* distortion.

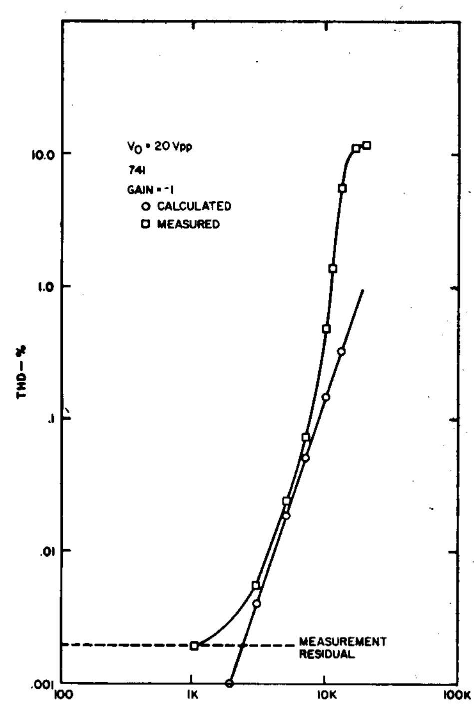


Fig. 32 — Calculated and measured distortion vs. frequency for a 741 at a gain of -10.

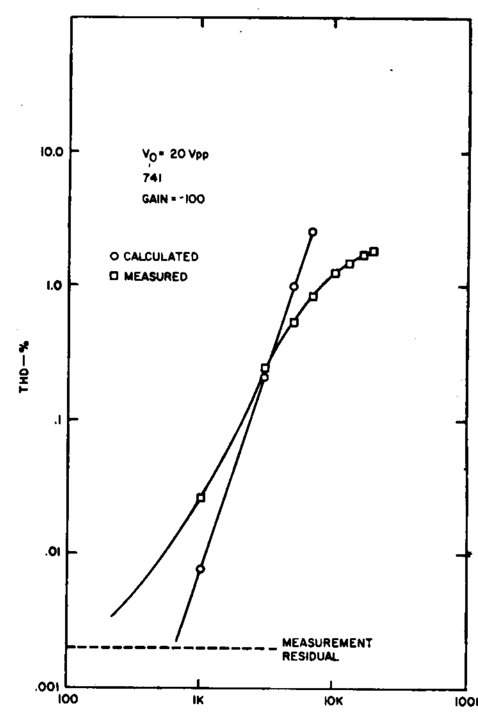


Fig. 33 — Calculated and measured distortion vs. frequency for a 741 at a gain of -100.

Equation (35) was developed specifically for the 741 op amp, which has a unity gain frequency (f_T) equal to approximately 1 MHz and a differential input stage consisting of four bipolar devices. A more generalized equation can also be developed which allows f_T to be a variable and which permits the number of input devices (n) to vary. This equation is

$$\text{HD (3rd)} = \frac{Vo^2}{12[n \cdot V_T]^2 \beta} \left[\frac{f}{f_T}\right]^3 \quad (36)$$

where n = number of bipolar devices (2, 4, 6, . . .), V_T = KT/q = 26 mV at 300° K, β = feedback factor, f_T = unity-gain frequency, Vo = output voltage, and f = frequency of fundamental.

Equation (36) reveals some characteristics of SID which were not evident from equation (35). First, it can be seen that increasing n reduces the distortion. This is due to a reduction in the curvature of the input transconductance curve (i.e. less change in g_m for the same current change) as n increases. Unfortunately, practical limitations usually require n to be 2 or 4 at most, so increasing n has a limited usefulness in reducing SID. Second, equation (36) shows the strong effect of the unity gain frequency on SID. Increasing f_T by a factor of 3 results in a distortion reduction of almost 30 dB! Clearly, f_T is a highly important parameter in improving SID. However, it is important to make the close connection between f_T and the SR limit. As pointed out by Solomon [21, 24] and others, for the 741-type circuit topology with bipolar input devices, f_T is proportional to the SR limit. This relationship is shown below

$$SR = 2\pi f_T(4V_T). \quad (37)$$

Therefore, improving f_T produces a proportionate improvement in the SR limit, which reduces SID.

Results of SID Calculation And Comparison with Measurements

The demonstrated accuracy of (35) and the generalized form in (36) in predicting harmonic distortion in a 741 amplifier leads to some useful conclusions concerning slew induced distortion.

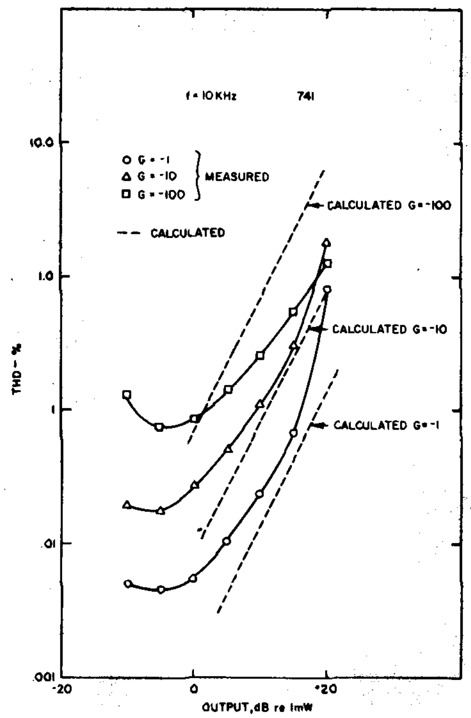


Fig. 34 — Distortion vs. output level for a 741 at various gain levels.

1) It means that slew induced distortion can be modeled and calculated with closed-form expressions, based on Volterra series principles.

2) It shows that slew induced distortion is increased by the input signal slope (SS) and the sharpness of the transconductance curve. It also shows that SID is decreased by more feedback and by a higher gain-bandwidth product.

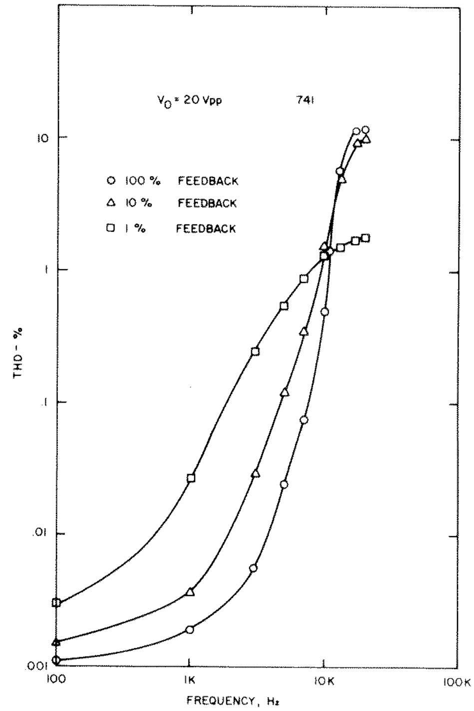


Fig. 35 — Distortion vs. frequency for a 741 at various feedback conditions.

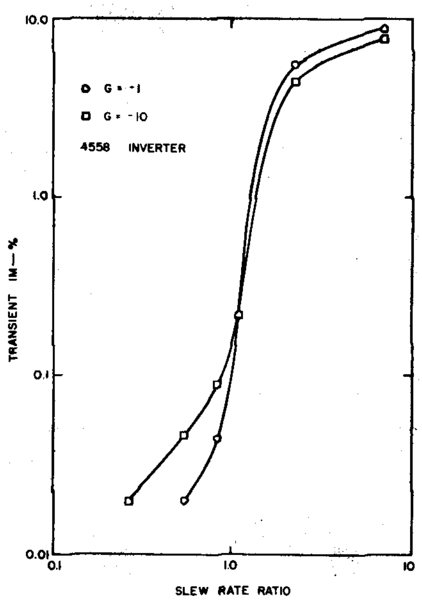


Fig. 36 — Transient intermodulation distortion vs. slew rate ratio for a 4558, operated inverting at two gain levels.

3) It demonstrates that since the slope of a constant amplitude sine wave is proportional to its frequency, that SID (or DIM, as in the sine-square test) should vary as the *cube* of the input SS. This is confirmed by the data in Figs. 20 and 24 that show the variation of DIM with SS is a cubic relationship.

4) It shows that increasing a device's slew capability, without adding additional nonlinearities (like slew enhancement), will reduce slew induced distortion.

The Effect of Feedback for SS>SR

Present TIM theory suggests that feedback increases distortion. Our measurements and calculations show that, at least for signal conditions *below* the slew rate limit (SR ratio <1), that feedback reduces distortion. The overall effect of feedback on distortion (for a constant slew rate capability) is shown by our data to depend on whether the SS is less than or greater than the SR limit. For SS<SR, increasing feedback reduces distortion. For SS>SR, increasing feedback increases distortion. There is a crossover point around SS=SR where feedback has a minor effect on distortion. These trends are evident in the THD plot of Fig. 35 and the sine-square (TIM) plot of Fig. 36. It should be remembered, however, that for distortion-free performance the SS must be less than the SR, and if this criterion is met, feedback can generally be relied on for distortion reduction. Operating an amplifier with the SS>SR is simply not a realistic consideration for high-fidelity reproduction. Some discussion and experiments of the next section will clarify these points further.

Designing for Minimal SID or TIM

We have now reached a point where the factors which govern the behavior of the SID mechanism have been discussed in principle. However, the discussion thus far has been largely focused on behavior as viewed from outside an amplifier or how to characterize it in terms of SID.

Perhaps more important is how to design an amplifier from the ground up for minimum susceptibility to SID or TIM. This section focuses on these aspects of the situation and develops techniques which can be used to predictably model circuit performance.

We will begin the discussion by returning to a two-stage amplifier model, shown in Fig. 37, which is similar in many regards to Fig. 5a of Part I or to Fig. 27 above. This two-stage circuit will now be used to develop a general topology which can be used to model amplifier performance and also dramatically illustrate the TIM and SID phenomenon.

A circuit topology similar to Fig. 37 was described 10 years ago in a classic paper by Solomon [24] et al. This paper contained a number of defining behavioral relations, which are not only historically important, but are also applicable to amplifiers of this type in general [47, 64].

A basic point which should be appreciated with regard to this two-stage amplifier is that one can actually design it to yield a given overall gain-bandwidth for an *infinite* set of combinations of stage 1 and stage 2 gains. The key question is, does it matter whether stage 1 or stage 2 furnishes the bulk of the gain? For herein lies the answer to the entire TIM and SID problem. In other words, how should the gain be partitioned between the two stages for best overall performance? Before we plunge into the equations which govern this, perhaps some discussion would be helpful towards insight.

We have already established by (14) that the SR which will be seen at Vo is set by I_K and C1. However, we also know that to increase SR we cannot just arbitrarily increase I_K or decrease C1, because of stability reasons. We must also decrease g_m simultaneously with either of these measures to maintain stability. In general, a lower g_m implies less gain in stage 1, i.e. the stage can accept greater input error signals ΔV before the saturation which results in TIM and/or SID is reached. Thus, it can be said that *to maximize SR in a given bandwidth, the stage preceding the integrator of a two-stage amplifier design such as this must have a low g_m and high I_K.*

Solomon expressed this as a *low* g_m/I_k ratio in [24] and [21], and it has also been expressed as a *high* I_k/g_m ratio by Gray and Meyer in [22]. The latter form allows an expression to be written which directly describes the amplifier's maximum input-voltage capability or dynamic range. This is the voltage which, when exceeded, will result in slewing. It is simply

$$Vth = \frac{I_K}{g_m}. \quad (38)$$

Others have termed this the input-voltage dynamic range [50]; however, the meaning is similar.

A greater application for how these relationships function may be obtained by examining two representative IC amplifiers with dissimilar Vth's. These types are used as examples because they are externally compensated and readily available. This allows convenient experimental duplication. A 301A amplifier (or 741, as noted above) has a g_m of

$$g_m = \frac{I_K}{4V_T}. \quad (39)$$

This equation can be expressed in terms of I_K/g_m or Vth, as

$$V_{th(301A)} = \frac{I_K}{g_m} = 4V_T. \quad (40)$$

Since V_T = 26 mV at room temperature, a useful approximation of (40) is

$$V_{th(301A)} \cong 0.104\ V. \quad (41)$$

Thus, a peak input voltage of 104 mV to a 301A (or 741) will cause it to slew.

To turn to another amplifier type, a representative FET input device is the TL070 (or TL080) which has a g_m of approximately

$$g_{m(070)} \cong 1.5\ I_K. \quad (42)$$

If this relation is expressed in terms of Vth, it becomes

$$V_{th(070)} = \frac{I_k}{g_m} = 0.67\ V. \quad (43)$$

As can be noted by comparison of (41) and (43), the TL070 FET achieves a Vth more than six times that of the 301A bipolar for similar conditions, This, for a comparable bandwidth, produces a higher SR. For example, for a 1 MHz bandwidth condition, the TL070 has a 4.3 V/ μS SR (Cc = 47 pF), while the 301A is only 0.67 V/ μS (Cc = 30 pF) [31].

For the amplifier model under discussion, a relationship can also be drawn between Vth, SR, and gain-bandwidth product (GBP) similar to that expressed in [24]. We use the more general GBP, rather than f_T, since GBP can often exceed f_T. Also, f_T is usually taken to mean the unity-gain crossover frequency and implies unity-gain stability. This is not always a requisite. An expression for SR in these terms is

$$SR = \frac{(V_{th}\ 2\pi\ GBP)}{10^6} \quad (44)$$

where SR is in V/ μS, Vth in volts, and GPB is the gain-bandwidth product (Hz) *at audio frequencies.* (The relevance of this equation to the subject of TIM and SID is fundamental. Although first described by Solomon and others [24], the authors would like to document that this relationship's importance to *audio amplifier* performance has been previously noted in letters to the A.E.S. by R. Cordell of Bell Labs, 9/77, and B. Olsson of Xelex AB, 11/77 and 2/79.)

This relationship clearly demonstrates that SR is directly proportional to Vth and GBP for this model. However, the caution should be extended that it does not apply universally. Two particular exceptions are some feed-forward amplifiers and slew-enhanced circuits such as IC type 531. In the case of a feed-forward type, such as the 5534, Vth is not

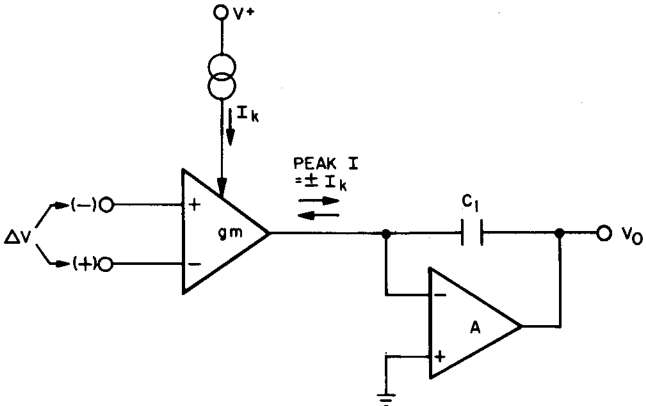
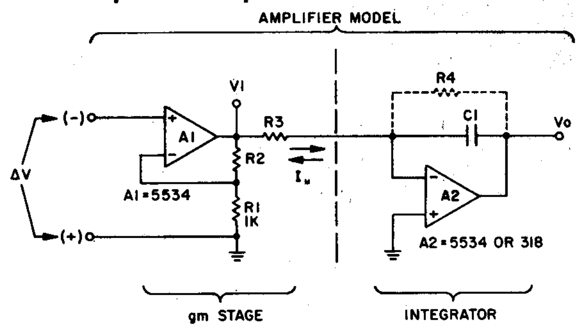


Fig. 37 — Two-stage transconductance-integrator model of a practical amplifier.



$$g_m = \frac{\Delta i}{\Delta V} = \left(\frac{R1+R2}{R1}\right)\left(\frac{1}{R3}\right) \quad (45)$$

$$I_M = \frac{V1(max)}{R3} \quad (46)$$

$$V_{th} = \left(V1(max)\right)\left(\frac{R1}{R1+R2}\right) \quad (47)$$

$$SR = \frac{I_M}{C1} = \frac{V1(max)}{R3\,C1} \quad (48)$$

$$f_p = \frac{SR}{2\pi V_{op}} = \left(\frac{V1(max)}{R3\,C1}\right)\left(\frac{1}{2\pi V_{op}}\right) \quad (49)$$

$$GBP = \frac{g_m}{2\pi C1}\ (50) = \left(\frac{R1+R2}{R1}\right)\left(\frac{1}{R3}\right)\left(\frac{1}{2\pi C1}\right) \quad (51)$$

$$f_o = \frac{1}{2\pi R4\,C1} \quad (52)$$

Fig. 38 — Synthesized two-stage amplifier model.

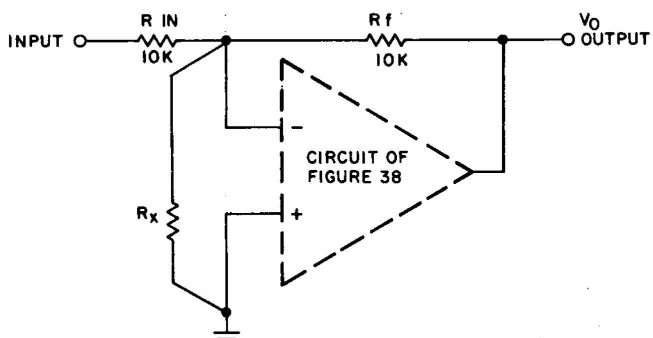


Fig. 39 — Test circuit for synthesized model.

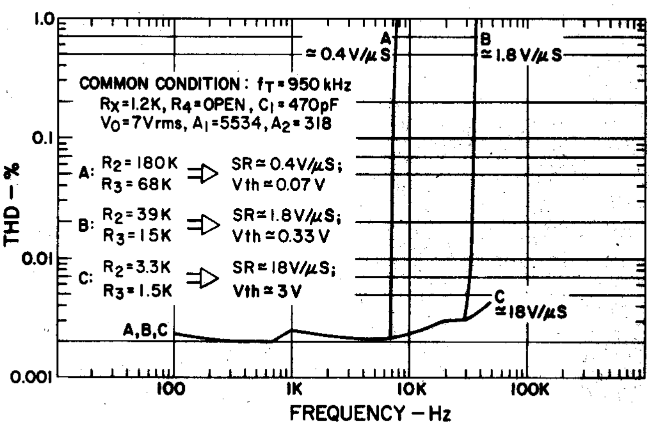


Fig. 40 — THD vs. frequency of the synthesized 741 op-amp model for various rate slew conditions (Test 1).

altogether a straightforward predictor of SR, as its Vth of 52mV and f_T = 10 MHz predicts only a 3 V/ μS SR. However, the GBP of this device is actually 22 MHz at audio frequencies — if this figure is used in (44), the SR predicted is 7 V/ μS, which agrees reasonably well. An important point is also that one must *not* be misled into the belief that slew-enhanced devices, which can show large voltages for Vth, lead directly to quality results. As has been shown previously, such amplifiers must be treated individually, as their dynamic input nonlinearities makes them special cases.

The relationship described by (44), while certainly an important one, can be erroneously misinterpreted. For example, it should not be interpreted to mean that *only* a very high Vth is fundamentally the route to high SR and thus low TIM. As (44) clearly shows, raising GBP (where allowable) achieves a similar result, and a practical example is the amplifier compensated for a higher noise gain (and thus GBP), such as the 301A of Fig. 11 (Part II). Such an example illustrates a *low* Vth device (the 301A) achieving a *high* SR. Another example is the 5534, a high GBP device, but with a very low Vth, only 52 mV! And, it should be noted, sufficient GBP must be present to result in a useful final closed-loop bandwidth.

The important thing to be remembered for this relationship is not totally Vth or GBP in absolute terms, but their *interrelationship,* which in many cases can be manipulated to achieve a high SR. The concept of a high Vth is, of course, most important when one is attempting to maximize SR *with a given GBP,* for as (44) shows, it is the only way it can be done with this type of circuit topology.

Experiments Which Demonstrate The Principle

A very cogent demonstration of the just described relationships can be made by synthesizing a two-stage amplifier model and subjecting it to various feedback and open-loop performance combination.

The circuit used for a series of these experiments is shown in Fig. 38 and is actually composed of two local-feedback IC op amps, which together comprise the model. A1 performs the function of a g_m input stage, converting the input voltage ΔV into a proportional current in R3. A2 performs the function of the integrator. Actual devices used for the experiments to be described were the 5534 for A1 and either a 5534 or 318 for A2. The devices used must, of course, have an inherent SR in excess of that which will be demanded by the model's operating conditions, as well as low distortion. These factors, combined with the local feedback, yield an amplifier with virtually ideal characteristics (even without overall feedback) as any nonlinearities are strongly suppressed.

A series of performance defining equations are included in the figure, and these can be manipulated with a great degree of freedom (another reason for using a model such as this, in fact). Some comment on these relations is in order before they are put to use, though.

Transconductance of the A1 stage is defined as

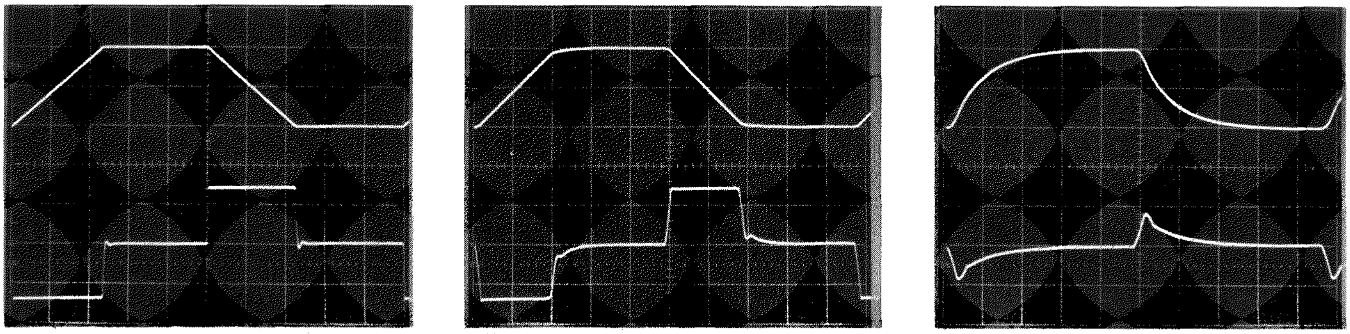
$$g_m = \left(\frac{R_1+R_2}{R_1}\right)\left(\frac{1}{R_3}\right) \quad (45)$$

Maximum output current, (I_m), is defined simply by the clipping voltage limit of A1, V1 (max) divided by R3, or

$$I_m = \frac{V_{1(max)}}{R_3}\ . \quad (46)$$

I_m, the peak output circuit, is analogous to I_K of Fig. 37, in that it sets the SR. It is slightly different in this case, due to more design freedom.

It is important to note that these two relationships are not exactly equivalent to those associated with Fig. 37. For example, the g_m of Fig. 38 can be set independent of I_m (if desired), and I_m can be set independent of g_m (if desired). This extra flexibility and the use of a voltage amplifier to produce V1



A B C

Fig. 41 — Transient performance of synthesized op-amp model with various slew rates to a 20-V p-p square wave of various frequencies. Top traces are outputs, bottom traces error voltages. A, SR = 0.4 V/ μS, 5 kHz; B, SR = 1.8 V/ μS, 20 kHz; C, SR = 18 V/ μS, 50 kHz. (Scales: All, 10 V/cm; A, 20 μS/cm; B, 5 μS/cm; C, 2 μS/cm.)

yields a direct monitor of the conditions in the input stage. A standard g_m input stage does not allow voltage monitoring of error signals.

Because of the above, Vth in this circuit is simply

$$Vth = V_{1(max)} \frac{R_1}{R_1+R_2}. \quad (47)$$

As this expression shows, Vth is simply the output overload voltage of A1, divided by the gain set by R1-R2.

The remaining performance equations are simply derived from combinations of others; as the figure shows

$$SR = \frac{V_{1(max)}}{R_3C_1} \quad (48)$$

$$fp = \left(\frac{V_{1(max)}}{R_3C_1}\right)\left(\frac{1}{2\pi V_{op}}\right). \quad (49)$$

Gain bandwidth product (GBP) follows from (8)

$$GBP = \frac{g_m}{2\pi C_1}. \quad (50)$$

Substituting g_m as described by (45), this becomes

$$GBP = \left(\frac{R_1+R_2}{R_1}\right)\left(\frac{1}{R_3}\right)\left(\frac{1}{2\pi C_1}\right). \quad (51)$$

Open loop bandwidth (in the presence of R4) is

$$fo = \frac{1}{2\pi R_4C_1}. \quad (52)$$

Without R4, it is reasonable to regard A2 as a near-ideal integrator, in which case fo is well below the audio range for practical values of C1, and the gain-bandwidth product is constant throughout the audio range, as set by (51).

Test Results

The first test (Test 1) performed on the model was to synthesize a standard 741 op amp in terms of GBP and manipulate it for differing SR. The results should show very linear behavior up to fp, and a hard limit or sudden distortion rise as slew limiting is reached. Conditions were set up for a unity signal gain inverter, with a noise gain of 20 dB, using the test circuit of Fig. 39.

Figure 40 shows the results of Test 1 for a THD swept-frequency test, at an output of 7V rms. Conditions A, B, and C are approximately 0.4, 1.8, and 18 V/μ S respectively. The different circuit conditions to yield these SR are noted. As should be noted, since GBP and the feedback conditions are identical for all three of these tests, the only variables are SR and Vth.

As can be noted from the A and B curves, these conditions produce a sudden distortion increase when the SS of the test signal equals the amplifier SR. The high SR of condition C prevents the limit from being reached, for any test condition. Note that Vth increases, going from A to C, in the same proportion as SR.

For a case of transient signal condition, the photos of Fig. 41 show how this same amplifier behaves for the three conditions set down in Fig. 40, but with a different method of measurement.

Figure 41A shows waveforms for the "A" test condition (SR = 0.4 V/ μS) for a signal condition of a 5-kHz, 20-V p-p square-wave input. The top trace shows the Vo waveform, which clearly resembles a 741 – type response (31, 38), changing 20 V in over 40 μS. Inside the loop, the error voltage V1 is shown at the bottom. Here it is seen that V1 saturates negative, then positive, for the corresponding (+) and (-) slew intervals, respectively. It is clear from this photo that the slewing evident in Vo is a result of saturation in V1.

Figure 41B shows waveforms for the "B" test condition (SR = 1.8 V/ μS), with a 20-kHz, 20-V p-p square-wave input. At the top, the Vo waveform shows that slewing is present, as is evident by the linear (+) and (-) slopes. This is confirmed by the V1 waveform, which again indicates saturation of the 1st stage for these corresponding times. This is similar to Fig. 41A, but the difference is that for this higher SR condition, the slewing intervals are simply shorter (note scale factor differences — do not be misled by same *general* waveshape).

Figure 41C is very interesting, because it demonstrates that a sufficiently high SR and Vth can completely prevent saturation of the first stage and maintain operation within the small signal region entirely. Conditions of these photos are an SR of 18 V/ μS. However, the feedback conditions described above in conjunction with the 20-dB noise gain result in an amplifier closed-loop, small-signal bandwidth of 95 kHz. This in turn is equivalent to a single-pole, low-pass filter with a time constant of 1.7 μS. For a 20-V p-p output from this filter (the amplifier), the maximum signal slope is 12 V/ μS.

For Fig. 41C, the signal input is a 20-V p-p 50-kHz square wave, and it can be noted that there is no slewing evident in Vo. The waveform is exponential in shape with a risetime of about 4 μS — consistent with the small signal relationships.

That slewing is not present is also confirmed by V1, which shows that the error voltage remains below the clipping level. Note that the highest amplitudes of V1 occur at the peak SS of Vo or at the transition points of the square wave.

This particular test confirms in another way the point made in Part I of this series, that slewing can be prevented by maintaining the amplifier small-signal bandwidth at a lower frequency than the power bandwidth. In 41C, fc is 95 kHz, but fp is 290 kHz, and no slewing is evident.

With this same model, experiments were also conducted to examine the sensitivity of the amplifier to open-loop bandwidth (fo). Test two conditions were commonly set up as described in Fig. 42, which resulted in an SR of 1.3 V/ μS and an f_T of 540 kHz. For this test circuit with R4 present at

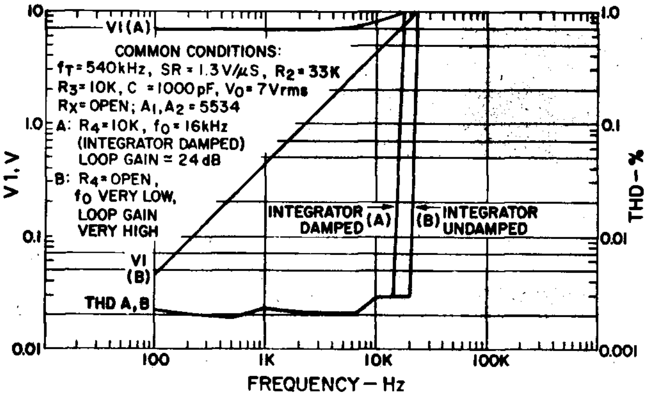


Fig. 42 — THD and error voltage vs. frequency of the synthesized 741 op amp model for different open-loop gain conditions (Test 2).

10K, fo becomes 16 kHz and the open-loop gain is 30 dB. With Rx open, the feedback is then 24 dB. With R4 open, the circuit becomes a classic op amp, with a very high open-loop gain and fo very low. Note, however, that *GBP remains unchanged for either condition.*

For condition A, where R4 is 10K, THD curve A indicates that slew limiting is reached at 18 kHz. V1 (A) is a plot of the rms error voltage versus frequency. Since it is essentially flat with frequency, it is testimonial to the wide open-loop bandwidth. Note that V1 increases to its clip level at 18 kHz, coincident with the slew rate limit point.

The B condition shows corresponding results with R4 removed, and the most obvious difference is the (apparent) increase in fp. Error voltage V1 (B) now increases 6 dB per octave with frequency, the inverse of the integrator's gain rolloff — what is necessary to maintain a flat output versus frequency for the overall circuit.

The *apparent* increase in SR for condition B is not an increase for this condition, but rather reflects a less than potential maximum SR *for the A condition.* This is so because the 10K resistor loading the integrator absorbs a portion of the charging current available to Cl for slewing.

These points are also brought out in the square-wave photos of Fig. 43. This shows response of the circuit of Fig. 42 to a 5-kHz, 20-V p-p square wave for conditions A and B.

For these test conditions, the transient performance is shown in Fig. 43. The slewing in Vo shown in 43A shows a quasi-linear ramp or a combination of ramp and exponential waveform caused by R4. Since R4 constrains the open-loop gain to a relatively low value, this is also reflected in the large error voltage shown in V1 (bottom).

The voltage V1 is clipped for the slew intervals (as expected) but also shows a very large potential (10 V) for the steady = state waveform positions. This excessive error voltage reflects a relatively large gain error for this circuit.

Figure 43B shows the Vo and V1 response for the same input drive but with R4 removed or condition B. Note that in 43B the slewing intervals are shorter and linear, as would be expected due to the constant and larger C1 charging current available. The error voltage shown in V1 is much lower in the steady-state periods, reflecting the increased gain available in the integrator. The low gain error is also reflected (more subtly) in the greater amplitude in Vo, compared to Fig. 43A.

This test indicates that, by both THD and transient response tests, there is no inherent advantage to a wide open-loop, small-signal bandwidth. By contrast, there are definite disadvantages to the constraint such operation can place on amplifier characteristics, such as limited LF loop gain and also some sacrifice in SR. And, while it is not apparent from this particular experiment, loading an integrator stage in a conventional amplifier will usually degrade the open-loop distortion characteristics.

Predicting A Non-Slew-Limited Response

We are now at a point where the information developed can be merged into a set of relationships useful in designing a *non-slew-limited* amplifier or an amplifier which is free of SID and TIM, by definition. This evolves in a fairly straightforward manner from the relations just discussed.

A non-slew-limited amplifier is simply one which *cannot* be made to slew for any signal input level below that which causes *amplitude* clipping. Input waveform shape is unrestricted and may include all waveshapes up to and including square waves. The square wave (as discussed in the sine-square box of Part II) is the most rigorous test to which an amplifier can be subjected because of its very high SS (infinite, for an ideal square wave). Therefore, if an amplifier can be proven to be free of slewing distortion for a square-wave test for all signal amplitudes in its linear range, it is by definition non-slew limited and will be largely free from SID or TIM problems.

All amplifiers will have by design a small-signal bandwidth, fc. This bandwidth will either be determined by the feedback configuration or an input pre-filter. The amplifier will then band limit a square-wave input signal to a bandwidth of fc. For simplicity at this point, we will assume this to be a single pole rolloff. For such a filter response it can be shown [33, 67, 70] that the signal slope of the resulting band–limited–output square wave is

$$SS_{(sq)} = \frac{2\pi V_{pp} f_c}{10^6} \qquad (53)$$

where Vpp is the peak-to-peak amplitude at the filter output, fc is the small-signal bandwidth, and SS is in V/µS.

That this signal slope is much higher than a sine wave at fc (passed through the same filter) can be shown by the relation of the two slopes. A sine wave at fc will be down by 3 dB

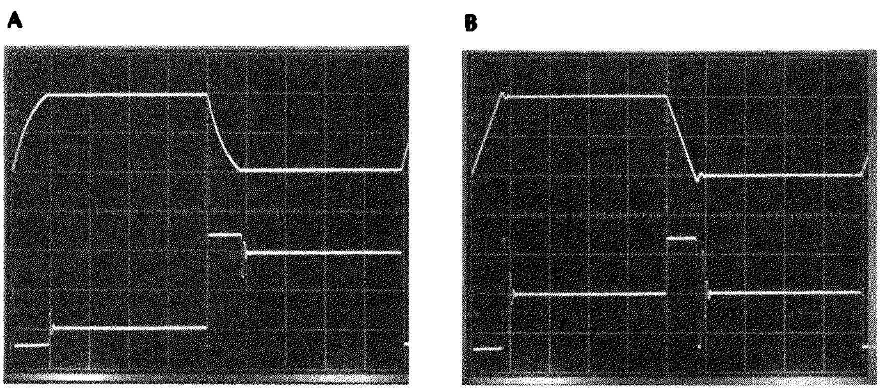


Fig. 43 — Transient performance of synthesized op- amp model with different open-loop gains to a 20-V p-p, 5-kHz square wave. Top traces are outputs, bottom traces error voltages. A, R4 = 10k; B, R4 = open. (Scales: 10 V/cm, 20 µS/cm.)

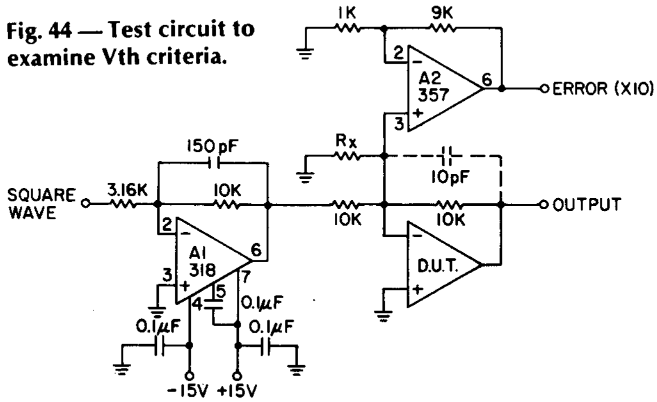


Fig. 44 — Test circuit to examine Vth criteria.

in amplitude, which can be expressed by modifying equation (1) by multiplying it by $\sqrt{2}/2$, yielding

$$SS_{(sine)} = \frac{\sqrt{2}\pi V p f c}{10^6}\,. \qquad (54)$$

Equations (53) and (54) can be combined to show their ratios as

$$SS_{(sq)} = 2\sqrt{2}\, SS_{(sine)}\,. \qquad (55)$$

Since this is nearly three times the signal slope of a sine wave at the frequency fc, it is clearly a more rigorous test. That it is the most rigorous test comes from the fact that the SS of the unfiltered square wave is infinite. It is clear then that an amplifier which passes a square-wave test without nonlinear distortion appearing in the output tends to be an optimum design. The question now arises, how can this be guaranteed?

We already know that to guarantee freedom from slew limiting we must, as a minimum, guarantee that the amplifier SR is in excess of the output SS for all possible signal conditions. For the non-slew-limited amplifier, this will encompass the signal slopes of square waves up to the rated output. We can set up a criterion to provide this with only a few parameters. Initially, let us consider a conventional feedback amplifier which follows the relationships discussed for Vth, SR, and GBP. By general feedback theory, we can express the bandwidth of this amplifier as

$$fc = GBP\ \beta \qquad (56)$$

where fc is the small signal bandwidth, GBP is its gain-bandwidth product, and ß the feedback factor. For this initial part of the discussion we will assume no other filtering, and the amplifier alone determines the bandwidth, as just outlined.

To guarantee no slew limiting, we desire that SR≥SS. To provide this, we can write an inequality, substituting the appropriate equivalents for SR and SS, as they pertain to this amplifier. SR is as described by (44), and SS by (53). The inequality is

$$\frac{2\pi\, Vth\, GBP}{10^6} \geq \frac{2\pi\, Vpp\, fc}{10^6}\,. \qquad (57)$$

With simplification, we can express this in terms of Vth as

$$Vth \geq \frac{Vpp\ fc}{GBP} \qquad (58)$$

Equation (58) gives us an expression for a minimum Vth, but we can further simplify it by substituting (56), which yields

$$Vth \geq Vpp\beta. \qquad (59)$$

The rather simple appearance of this expression may hide its rather profound implications. Since Vppß is in fact equal to the peak-to-peak input voltage, this relationship states that Vth should be in excess of the maximum pp input amplitude. In other words, the input stage (alone) will not overload when driven with a full-scale input signal [47, 67].

That the criterion works can be illustrated with some data just presented. In test 1, condition C it was observed that the experimental amplifier did not slew limit when subjected to a full-amplitude square-wave input. For condition C, Vth was 3V and the SR was 18 V/ μS. If a minimum Vth is calculated from (59) for this amplifier, it is found to be 2V. Therefore condition C satisfies (59), since 3V>2V.

On the other hand, if condition B is examined, it will be noted that Vth is only 0.33 V, and slew limiting *did* occur (Fig. 41B). Here the criterion was violated; i.e., 0.33V< 2V.

Another example, more in the line of a real amplifier, was the variable-feedback amplifier from Part I, discussed in Figs. 3 and 4. If Figs. 4a, 4b and 4c are re-examined, it will be noted that slew limiting is evident in condition A and some in B. Condition C is a non-slew-limited case.

Since the gains in this case were 20, 40 and 60 dB, respectively, ß is correspondingly 0.1, 0.01, and 0.001. As the output level is 20 V p-p in all cases, it can be noted that conditions A and B violate the minimum Vth criterion, which says that Vpp should be less than the 301A's Vth of 0.104 V. In condition C, the criterion is satisfied, and no slew limiting is evident.

It may already have occurred to some readers that this criterion is a most restrictive one, as it dictates *very low feedback factors* to eliminate slew limiting *in the case of low Vth amplifier stages.* Inasmuch as all directly coupled, undegenerated bipolar-transistor differential-amplifier pairs have a Vth of 0.052, this can quite logically explain TIM and slew limiting possibilities in power amplifiers, where Vpp may be upwards of 70 V.

It is interesting to plug typical power amplifier numbers into the relationship of (59) to see what results. A 100 W-into-8-ohm amplifier with a gain of 20 (26 dB) has a Vpp of 80 V and a ß of 0.05, which results in a required Vth of 4 V . . . clearly many times in excess of the 0.052 V resulting when an undegenerated bipolar differential pair is used in the input stage.

As a historical comment, the vacuum tube, still favored by many, has a Vth on the order of 3 V, for a typically used type

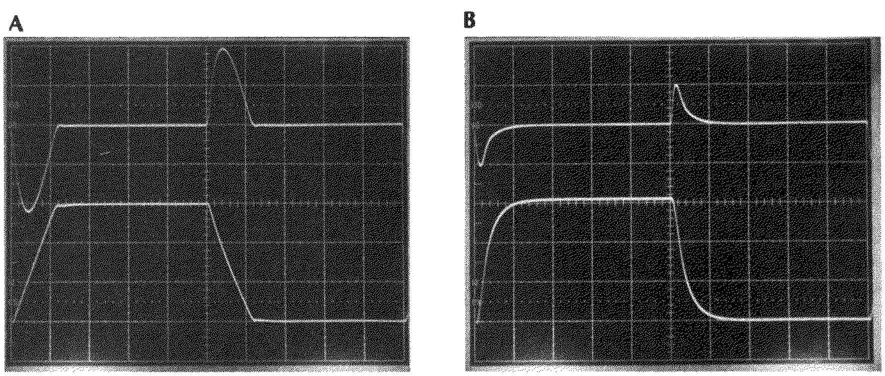


Fig. 45 — Transient response of a 301A, operated inverting with unity-gain compensation, Cc = 33pF, to 20-kHz square wave filtered at 100 kHz. Top traces are error voltages, bottom traces outputs. A, slew-limited response, and B, non-slew-limited response. (Scales: 5 μS/cm both; A, 0.5 V/cm top, 2 V/cm bottom; B, 0.1 V/cm top, 0.5 V/cm bottom.)

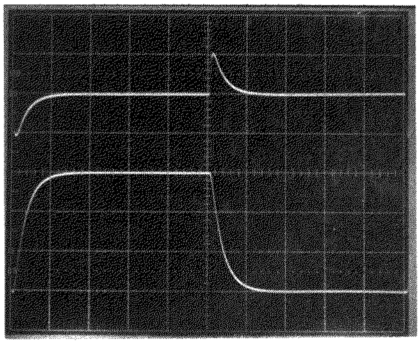


Fig. 46 — Transient response of a 301A, operated inverting and adjusted for slew suppression, Rx = 1.2 k, Cc = 5 pF. Top trace is error voltage, bottom trace is output. (Scales: 5 μ S/cm for both; 0.05 V/cm top, 2 V/cm bottom.)

such as the 12AU7. Viewed in this light, it is quite easy to see why a vacuum-tube design is much less susceptible to SID type problems; not only did they have less feedback in general, but they could also easily accommodate much larger inputs without first-stage clipping (47).

Viewed in just the above light, it is rather easy to conclude that the transistor audio power amplifier cannot be made to work. If, for example, we were to manipulate ß to satisfy (59) for the 100 W amplifier, using a Vth of 0.05, ß becomes 0.000625 (or less), which corresponds to a gain of more than 60 dB! While this probably is a completely impractical signal gain, it is possible to use special compensation "tricks" such as input compensation [25, 31, 63], which provide a low ß, but at elevated frequencies (above the audio range).

Of much greater interest are practical techniques which can be used to design an amp for no SID, *without* having heavy restrictions placed on the feedback loop. This can be done by separating the filtering and amplification functions, so that each can be optimized separately.

If an amplifier is preceded by a low-pass input filter with a cutoff frequency of fc, the filter-plus-amplifier combination can control the output signal slope with relative independence of the feedback factor. There are still restraints upon the Vth (or Vpp) of the amplifier, however, they are lessened to a great degree.

For this discussion it is assumed that the amplifier operates linearly and its own natural cutoff frequency, as determined by (56), is sufficiently higher than that of the input filter so as to cause negligible interaction. For such a linearly operated system, the peak-to-peak output of the input filter can be scaled by the gain of the amplifier, and the SS resulting at the output is of the same form as (53), but the relevant Vpp is the rated output of *the amplifier.*

If we now write an inequality such that the amplifier SR is to be maintained greater than the output SS, it follows the initial development form to (58), which is repeated here

$$Vth \geq \frac{Vpp\ fc}{GBP} \qquad (58)$$

Written thus, it can be seen that as fc is lowered and GBP raised, the Vth required can be lowered. Within certain constraints, this allows considerably more design freedom. Like the previous relationship, this is one best understood by examining some performance which illustrates it functioning.

For an amplifier where Vth and GBP are fixed (as the 301A example of Part 1, Figs. 3 and 4), the only relief from the slewing problem is to decrease feedback in accordance with (59) until the criterion for Vth is satisfied. However, when we have control over GBP, we can manipulate things effectively to minimize slewing problems as we can by changing Vth.

A test circuit which can be used to demonstrate the relationship of (58) is shown in Fig. 44. Here A1 and the associated components form a 100-kHz single-pole filter, which drives the D.U.T., connected in an inverting circuit. This allows direct observation of the error voltage, thus this monitor shows directly when Vth is exceeded. The error voltage of the D.U.T. is buffered by A2, a high-speed FET amplifier, which furnishes a voltage gain of 10 to aid observation of low error voltages without loading the summing point. Rx is used to adjust the feedback of the D.U.T. test amplifier. A small (10 pF) feedback capacitor is used to minimize HF phase errors (which can obscure detection of slewing near threshold).

To check the validity of (58), a hypothetical amplifier stage was set up to pass a 6-V p-p output signal, after being filtered by the 100-kHz input filter. (Such a stage, for example, could represent the last stage of a preamplifier, and the numbers quoted are reasonable design figures.) A 301A compensated for unity gain with a resulting SR of 1 V/ μS and GBP of 1.5 MHz was used, with Rx open. The results for this device are shown in Fig. 45.

The bottom trace of this photo, 45A, is the output, which as can be noted is severely slew limited for the 6-V p-p level. The error voltage (top) is 1 V peak in level, well in excess of Vth, a confirmation that slewing is present in the output.

If (58) is an accurate predictor of slew suppression, it should be possible to adjust this stage to a point where slewing is not present.

If (58) is rewritten in terms of Vpp, as

$$Vpp \leq \frac{Vth\ GBP}{fc} \qquad (60)$$

we should be able to calculate a Vpp below which this is true, for this circuit. Equation (60), with the substitution of the appropriate conditions, indicate that slewing should disappear below 1.5 V p-p, the level where Vth is 0.1 V.

A photo for these conditions (displayed similarly) is shown

A B

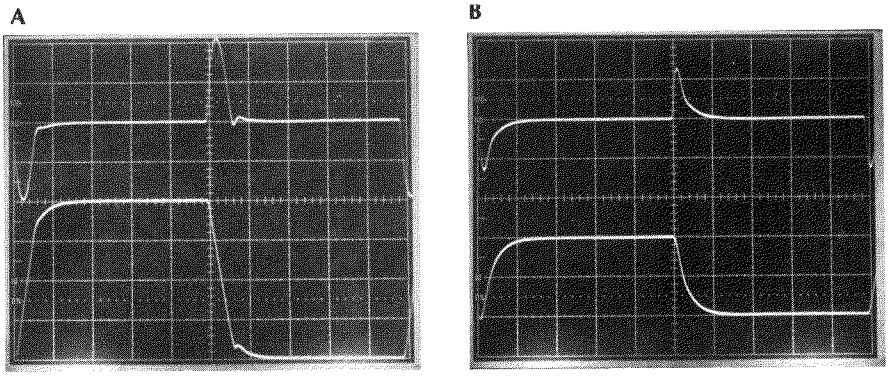


Fig. 47 — Transient response of TL070, operated inverting with unity-gain compensation, Cc = 33pF, GBP = 1.5 MHz, Vth = 0.67 V, to 20-kHz square wave filtered at 100 kHz. Top traces are error voltages, bottom traces outputs. A, slew-limited response; B, non- slew-limited response. (Scales: 5 μS/cm both; out puts both at 5 V/cm; error voltage, A, 1 V/cm, B, 0.5 V/cm.)

in 45B. As the output level and Vth indicate, slewing is just barely discernible in the output waveform (bottom). For levels below 1.5 V it will be absent; above 1.5 V it will appear with increasing degree, with increasing amplitude.

Equation 60 can also be used to adjust GBP to a point where higher output levels are possible without slewing. With the same 301A compensated with 5pF, its GBP became 10 MHz, which should allow the 6 V p-p output to be realized. For stability, Rx must become 1.2 K for this test.

The results, shown in Fig. 46, indicate that a 6-V output is realized without slewing. As can be noted, the error voltage is under 0.1 V (top) for this condition, indicating that operation is conservatively below the slew limit level. Equation 60 actually predicts a 10 V p-p output before slew limiting is reached.

Another demonstration of how the relationships of (58) and (60) operate is possible by using an amplifier with a radically different Vth to see if it predictably follows a similar pattern. This was done for a TL070 device, which for a similar compensation capacitance of 33 pF also has a 1.5 MHz GBP. However, due to its higher Vth of 0.67 V, the SR for this device and condition is 6.7 V/μS. As should be noted, these conditions produce a test amplifier with 6.7 times the Vth and SR over the 301A.

Figure 47A shows the output/error voltages for the TL070 compensated as noted for a 20-V p-p output. Slewing is evident in the output (bottom) and indicated by the 2-V peak error voltage (top) which is in excess of Vth. Equation (60) predicts that slew limiting should disappear below a 10-V p-p output, which is shown in 47B. Note that the error voltage is just over 0.6-V peak, and slewing is just barely noticeable in the output (bottom).

If this amplifier is adjusted for a higher GBP, as was done in the 301A case in Fig. 46, it shows a similar improvement. For this 10-MHz GBP condition, the output predicted by (60) would be 67 volts p-p or in excess of the supplies. The results at a 20-V level are shown in Fig. 48, and there is no slewing detectable at all.

It should be noted that these two examples do indeed demonstrate similar adherence to the relationship described. If the results are compared for conditions where the error voltage is at the Vth level, for example Figs. 45B and 47B, it can be noted that although the two output levels produced are different (due to different SR and Vth), *the error voltages are of a similar percentage of the output* or about 6.7 percent. This demonstrates that it is, indeed, possible to satisfy a common criteria (SR>SS) by different means, with similar errors by the different routes taken.

Another way of stating this is to rephrase an earlier statement, that Vth *in itself* is not a single totally important parameter—it is important to this subject to the extent it affects SR and input overload. The relationships set down in (58) and (60) are somewhat deceptive in this regard, as they do not contain an SR term. However, it should be remembered that these two relationships are *fundamentally based on an SR criterion* and, as such, contain terms which are useful towards manipulating or maximizing SR. In a very broad perspective, it should also be understood that it is incomplete to imply that input dynamic range, Vth, or other similar conceptual terms describe the entire situation in terms of a no-slew-limit guarantee, for they do not. As the experiments just described have demonstrated, even a low Vth amplifier can be effectively used. If its operating conditions are set up to provide an SR>SS, the obvious slewing distortion can be suppressed.

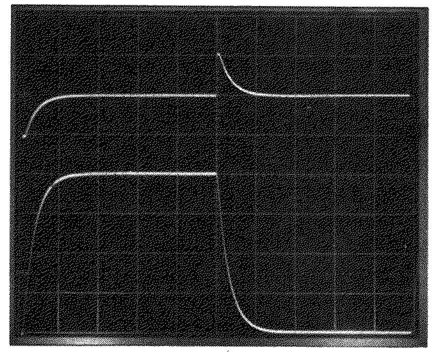


Fig. 48 — Transient response of a TL070, operated inverting and adjusted for slew suppression, Cc = 5 pF, Rx = 1.2 k. Top trace is error voltage at 0.1 V/cm, bottom trace is output voltage at 5 V/cm.

There is a great deal more which can be said about specific amplifier operating conditions and methods of suppressing SID by guaranteeing SR>SS. Unfortunately, however, the scope of all of these factors might be a complete article or series in itself. Therefore, we will limit comments on these points to the highlights at this time.

What the relationships just discussed show is that when the output of an amplifier stage is, by design, purposely confined to signal slopes less than the SR of that amplifier, the amp will not slew limit. Further, if SR is maintained greater than SS for all output levels up to (or above) the clipping level, the amplifier will not slew limit for any input level below clipping.

While this was demonstrated with a model consisting of a separate input filter followed by the amplifier under test, it also holds true when the filter is integral to the amplifier, i.e. the amplifier is an active LP filter. An amplifier can, in fact, be designed in this manner for slew suppression, as described by Leach [10]. However, the conversion of an amplifier to an integrator at high frequencies will usually result in more compensation being necessary for stability, hence there can often be little net improvement for this approach.

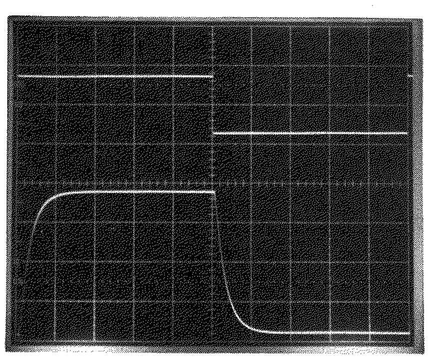


Fig. 49 — Transient response of a non-slew-limited amplifier design, loaded with 8 ohms, to a 10-kHz square wave. Top trace is input at 2 V/cm, bottom trace is output at 20 V/cm.

In practice, effective control and design freedom are also realized when the slope limiting filter is placed before the amplifier. This allows reduced compensation and a high SR in the amplifier, with complete control of maximum signal slope by means as simple as a single RC input section.

An example of a power amplifier design based on these principles is described in reference [71], and it is worth noting that a commercial design [72] following these principles has received some good marks from audiophiles and subjective reviewers. To illustrate the point that this amplifier is indeed a non-slew-limited design, a full-level output (80 W) square wave from it is shown in Fig. 49, along with the input square wave. It is clear that the response is small-signal-bandwidth limited only, and the 6 μS risetime does not, in fact, vary as a function of level.

The design techniques and experimental data described above for reduction of SS by prefiltering at the amplifier input have all been based upon single-pole, low-pass filters. While this type of filter has been shown to be quite effective for control of SS, and thus prevention of slew limiting, more sophisticated filter techniques are even more effective in reducing SS.

It has been shown [12, 66, 67, 70] that higher order filters are even more effective for reduction of SS, compared to a simple first-order type, for a given cutoff frequency. There are, of course, trade-offs to be made in comparing one to the other, considering the higher performance against the increased complexity. Also, the damping of the filter must be considered, as well as its frequency. However, the increased complexity of a second-order filter really depends on exactly how it is realized and may not in fact be prohibitive. For example, Leach has shown in [66] how the amplifier itself can be used as the active portion of the prefilter, without undue stability constraints, in what appears to be a practical and attractive topology. Further, in [70] it is shown that a second-order Bessel LP filter alignment will produce approximately 1/2 the SS of a single-pole filter for otherwise similar conditions. Unfortunately, time did not permit detailed experimentation with these techniques for this article, but they appear to have significant merit towards the reduction of SID effects.

Generally, the above discussion describes two alternate means which can be used to design a non-slew-limited amplifier and thus prevent SID and TIM. A logical question which may be raised is, do they yield equal results in auditioning? While we do not at this point have subjective response data to definitively answer this question, informal listening tests by one author (W.J.) tend to favor circuit topologies which are designed from a standpoint of equation (59), using linearized input stages, such as FET or degenerated bipolar devices. As time progresses, it is hoped that further listening tests will more clearly define the optimum choice between the two approaches.

Conclusions

In this article we have attempted to cover a quite broad topic from a multiplicity of viewpoints, in both discussion and analysis. These different techniques of analysis all indicate a common pattern of distortion in feedback audio amplifiers, which is a function of the ratio of signal slope to amplifier slew rate, a dimensionless parameter we define as SR ratio. When the SR ratio is less than unity, this distortion is suppressed; when greater than unity, strong nonlinear distortion products appear, which are subjectively objectionable.

Control of this distortion, which we call SID, can be achieved by maintaining linear amplifier behavior, with an SR greater than the highest SS, or stated in terms of SR ratio, an SR ratio less than unity. Since SS is both frequency and amplitude dependent, it follows that greater SR in an audio amplifier is required for higher voltage output stages, where the SS is highest.

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Control of this distortion can be exercised by appropriate selection of amplifier type, by specifying an SR sufficient to the application. In design, it can be achieved by providing a sufficiently conservative SR (on the order of 0.5 V to 1V/ µS per peak output volt) or by designing for a non-slew-limited response. A non-slew-limited amplifier has an inherent SR greater than its maximum possible output SS and will therefore never slew for any input signal, including square waves, or its SR ratio is guaranteed <1. It is characterized by frequency response which is small-signal-bandwidth limited, for any output below its clipping level. As such it has no major nonlinear distortion products due to slewing effects. Such an amplifier is also said to be TIM free and may be described in this context as well.

It is recognized that there is considerable controversy on the relative importance of TIM and SID, their audibility, and some of the relevant design criteria. For this discussion, it is not our purpose to dwell excessively on the relative importance of SID, its audibility or other factors which are often subject to opinionated views. What we seek to do is describe means to quantify and control this distortion mechanism, and basically this is the only main point being addressed.

The existence of the distortion mechanism is, of course, *not* a subject of debate, and like other distortions in amplifiers, knowledge of its behavior patterns is valuable to either the circuit designer or the informed user of audio equipment. We would, however, like to express caution with respect to certain alarmist commentary, for example those to the effect that low TIM or minimal SID is the magic elixir of quality audio. While this distortion source is quite important, so are many others. Once sufficient linearity and slew rate have been provided in a design, there may actually be little gained by boosting SR further (to far beyond that necessary). The *optimu* audio amplifier is best designed with *all* contributions to audible defects given proper perspective.

We appear to currently be immersed in a specifications race on the part of some manufacturers in this regard, which is not only unfortunate for the confusion it spreads (as to what is most important), but doubly so from the standpoint that if nonlinear techniques are being used to achieve high SR numbers, the user can actually pay a penalty in *higher* distortion!

Another specifications race practice appears to be the quotation of amplifier maximum output SS *for small signal condition* as its specified SR. If an amplifier is operating linearly in non-slew-limited conditions, the output SS for a fixed signal will linearly follow the output level, and at no point will it reach the true amplifier SR, which is, in fact, a limit. It is therefore erroneous or misleading to quote a maximum SS as an SR in such a case, as the *true* SR limit is never reached. In our opinion, while such an amplifier has real merit, it might more clearly and suitably be described in such terms as "maximum linearly reproduced SS" or the qualifier added that it is a true non-slew-limited design, as described in the text. Using the terminology of SR implies that the amplifier *can* be made to slew; if, in fact, it *cannot* be made to slew this should be clearly stated, for it is a point which distinguishes the design.

(In Part II on page 44 in July under "Comparison of Test Methods," we made the statement that the squarewave's *fundamental* amplitude was 12 dB larger than the sine wave's. The square wave *itself* is 12 dB larger in amplitude, as described in the sidebar.)

We hope this discussion has served to bring together some of the various issues involved so as to create a new perspective for the reader. We recognize that some of the points made in this article have been made elsewhere and acknowledge the work of previous authors. We believe that the extensive bibliography will be helpful to the reader to appreciate this material, and to tie older data in with the new material presented within this article.

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