Analog's Shrinking World

The Pros And Cons Of Surface Mount.

An obvious fact of life about the hectic world of electronic engineering that we live in is that it constantly becomes more so. At one time or another, everyone has wished for "the good old days" when life was simpler and our electronic hassles were less frequent. Of course, those good old days won't be coming back, no matter how hard we wish. We are just left to our own devices as how to best deal with this modern world of ours. Thus enters the topic(s) of this column.

Analog electronics has never been a piece of cake under any circumstances, and typically, it presents us with all sorts of steady challenges. There are the circuit design challenges, which deal with the initial concepts of a design to a certain specification, including hand calculations and/or simulations. Then, there is a breadboard phase, where the design is built up and tested in a lab environment, but usually within loose guidelines regarding a final form factor. The following prototype phase is intended to be very close to final form in size, shape and other physical/electrical factors, and may involve final environmental testing.

While various tools and other design aids have arisen to help expedite the various phases of the design process, these aren't the main focus of this column. Instead, as a broad general example of how the analog designer's life has become more complex, I'd like to talk a bit about some current trends in packaging. The revolution in printed-circuit board (pc board) packaging and design is driving our electronic systems, and quite hard. And, it seems to me that this drive is not always for the good; at least it is generally not always positive from an analog designer's perspective.

Take the surface mount (SM) craze for example, and the general rush to miniaturize and integrate everything. Many electronic components aren't necessarily improved by being shrunk to minimum size. For example, in SM vs. traditional leaded passive components, performance can be sacrificed in several ways. Power dissipation is an obvious one; it is unquestionably a challenge to get the heat out of a part when the only appreciable heat sinking is through two surface-mount leads. Although individual SM chip thin-film resistors are available, their stability/accuracy, while good, isn't up to that of the best leaded components. But thin-film arrays in SM can be quite good, as they take advantage of the natural ratio matching/tracking properties typically critical for analog gain stages.[1]

For capacitors, high-Q, low-dissipation-factor units are available in NP0 ceramic chips, but only in small sizes (≈0.01μF or less). So, if you need a high quality 0.1μF film capacitor for a filter or sample-and-hold circuit, you'll need to look very hard to find one in surface mount (and then it won't be as good as a leaded type). Surface-mount inductors are a real form and function mismatch, but nevertheless they, like many other parts, are fast being force-fitted into this component style.

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Active parts have seen a radical revision of packaging standards, with many standard ICs like op amps now going into SM compatible SOIC and even more tiny packages, such as the SOT-23. By contrast, familiar 8-pin DIPs may seem almost an anachronism! But, in these cases as well, smaller isn't always better, as a designer using these tiny packages definitely gives up power dissipation. Take an 8-pin package, for example. A DIP version has a thermal resistance of about 90 to 100°C/W, while an SOIC raises this by about a factor of 1.5, and a TSSOP by an additional 1.5X factor. If you go to the extremely small package size of the SOT-23-5, you are talking about a thermal resistance in a range of 300 to 400°C/W, which places rather severe constraints on the part's allowable dissipation.

Performance also can be affected directly and indirectly, as obviously die sizes are small simply to allow such packages, which means more simple, single-function circuits. But some aspects of a smaller chip size are good, i.e., the package's parasitics are lower, meaning better high speed amplifier performance, for one thing. The bottom line here is that more or less chip performance can be available to the end user in SM, dependent upon whether high speed or high dc precision is the primary design goal.

All-in-all, today's typical pc-board designs using SM parts have cramped the design freedoms of an analog designer in many ways. With pc boards typically being multilayer to accommodate largely the digital aspects, the analog subsystem gets to share this, with a big price paid in terms of difficulty in prototyping and troubleshooting. There is no clear-cut answer to address this serious issue, although careful DIP breadboarding, simulations, and lots of prior experience can be helpful.

It's also true that the constraints of SM parts bear little burden for a digital designer, where subtleties of passive component performance are rarely so critical. And, unfortunately, since digital designs outnumber analog by at least an order of magnitude, their requirements call the shots driving most new component developments. And, the analog design challenges get much greater as parts shrink and board densities/complexities increase. And so, the discussions above are best taken as an introductory "fact-of-life."

In truth, the analog designer needs all the help that can be mustered just to stay ahead of the game these days. While dealing with SM and pc-board design issues can certainly be challenging enough, this is but one of a number of vexing issues facing the analog technical types.

References:

1. See SM type "ORN" thin film series, Vishay Thin Film, 2160 Liberty Drive, Niagra Falls, NY, 14304; (716) 283-4025.

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