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Walt Kester
1993

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SECTION 8

AUDIO APPLICATIONS

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AUDIO PREAMPLIFIERS, LINE DRIVERS,
AND LINE RECEIVERS

Walt Jung

AUDIO PREAMPLIFIERS

8

Audio signal preamplifiers (preamps) represent the low-level end of the dynamic range of practical audio circuits using modern IC devices. In general, amplifying stages with input signal levels of 10 mV or less fall into the preamp category. This section discusses some basic types of audio preamps, which are:

■ *Microphone* - including preamps for dynamic, electret and phantom powered microphones, using both transformer and transformerless circuits operating from dual and single supplies.

■ *Phonograph* - including preamps for moving magnet and moving coil phono cartridges using a variety of topologies, with detailed frequency response analysis and discussion.

■ *Tape* - including preamp designs useful for a wide range of playback standards including NAB and IEC, covering various time constants/tape speeds.

In general, when working signals drop to a level of 1 mV, the input noise generated by the first system amplify-

ing stage becomes important for wide dynamic range and good signal-to-noise ratio. For example, if the internally generated noise voltage of an input stage is $1\mu\text{V}$ and the input signal voltage 1 mV, the very best signal-to-noise ratio possible is just 60 dB.

In a given application, both the input voltage level and impedance of a source are usually fixed. Thus, for best signal-to-noise ratio, the input noise generated by the first amplifying stage must be minimized when operated from the intended source. This factor has definite implications to the preamp designer, as a "low noise" circuit for low impedances is quite different from one with low noise operating from a high impedance.

Successfully minimizing the input noise of an amplifier requires a full understanding of all the various factors which contribute to total noise. This includes the amplifier itself as well as the external circuit in which it is used, in fact *the total circuit environment must be considered*, both to minimize noise and to maximize dynamic range and general signal fidelity.

AUDIO LINE DRIVERS AND BUFFERS

Audio line drivers and buffer amplifiers can take a wide variety of forms, which include single-ended and differential output drivers, as well as transformer isolated drivers. Within these general formats there are many different performance options, many of which are covered in this section.

Many op amps useful as video drivers and buffers also do well as audio driv-

ers, because of the high current output stages necessary for good linearity over video bandwidths.^[1,2] Some examples of video amplifiers which are useful for audio are the AD810, AD811, AD817, AD818, AD829, AD840 series, AD845, AD846, and AD847. Other types notable for either high or unusually linear output drives or other performance features useful in audio applications are the AD797, OP-275, and SSM-2131.

High Current Buffer Basics

As a preliminary to detailed application discussions, some basic circuit principles germane to high current buffers and drivers should first be considered. With output currents up to 100mA or more, "housekeeping" details of bypassing, grounding and wiring become even

more important than usual, and must be considered. These are briefly discussed here in the context of high current buffers, using the unity gain buffer circuit of Figure 8.39 as a point of departure.

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UNITY GAIN STAND-ALONE BUFFERS

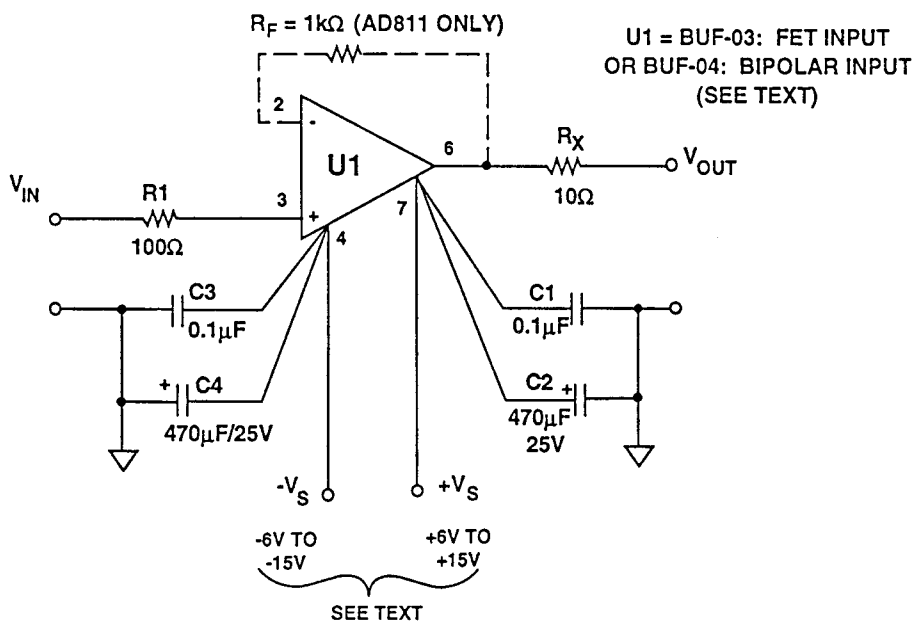


Figure 8.39

First, whichever IC is used for U1, close attention should be given to making buffer stages free from parasitic capacitances and inductances, at input, output, and supplies. Physical construction of buffer-drivers and other high current stages should be in accordance with high speed rules. A continuous copper ground plane is preferred, and circuit layout should be compact, with low capacitance around high-Z nodes. Signal and ground runs should be laid out with signal coupling and load current flow in mind.[3-6]

In addition, the power supplies should be well bypassed close to the high current supply pins. In Figure 8.39 this is indicated by the Kelvin connections of C₁-C₄ to the ±Vs pins of U1. This should be standard practice for all high current stages, and must be used for all the driver applications in this section.

As a minimum, local low inductance/low ESR RF bypass caps should be used within 0.25" of the device supply pins, shown as C₁ and C₃. These are preferably 0.1μF ceramic or other low inductance capacitor type. In addition, for high peak current loads, the high frequency bypasses are paralleled by local, short lead/large value, low ESR electrolytics such as C₂ and C₄, in a range of 470μF/25V and up. Note that capacitor ESR reduces in inverse proportion to electrical size and voltage rating, so larger size and/or voltage units help. These capacitors carry transient output currents, and should be aluminum electrolytic types rated for high frequency use, that is switching supply ones. Such capacitors tend to have low Q, and are thus less likely to cause power line resonances than are tantalum capacitors.

DC power management and dissipation are important with buffer ICs. For

example, the BUF-03 and the AD811 ICs can dissipate fairly large power levels even with light loading at supplies above ±12V, because the quiescent current of these devices is 15-18mA, relatively independent of operating voltage.

As a conservative rule of reliability, any IC with a power dissipation above 300mW should not be used without a heat sink. For buffer or driver circuits using more than 300mW, use the lowest thermal resistance package possible, and the appropriate heatsink (Thermalloy 2227 for the BUF-03 or other TO-99 ICs, or Aavid #5801 for the BUF-04, AD811 or other high dissipation 8 pin ICs).

Output resistor R_x in this circuit should be 10 ohms or more, to isolate the buffer from capacitive loading (more on this, below). For an extra safety margin against possible de-stabilization due to capacitive loads, make this resistor as high as practical. Input resistor R₁ is a "bullet-proof" parasitic suppression device, and may be required for stability with some amplifiers but it is not absolutely essential for those we have discussed.

Because of this stage's very high bandwidth, low phase shift, and low output impedance, fast buffers such as this can be used both "stand alone" just as shown, and as a more conventional "in loop" buffer as well, to minimize loading of a weaker, slower amplifier. For any modest output amplifier this is an obvious improvement, as raises the linear output to more than ±100mA (with the AD811 or the BUF-04), while maximizing linearity, preserving gain, and lowering distortion.

Operating in a pure stand-alone mode, THD+N tests on several buffers are

shown in Figure 8.40, for conditions of 10Vrms into a 600Ω load. The BUF-03, a design with no closed loop feedback path, shows a distortion for these conditions of about 0.15%. The BUF-04, a closed loop transimpedance design buffer, shows a very low distortion of about 0.004%. The AD811 transimpedance amplifier, externally configured as a unity gain follower with

$R_F = 1k$, shows an intermediate level of distortion, just under 0.01%. As a choice among these types, both the BUF-04 and AD811 are capable of more than $\pm 100mA$ of output, and have input currents on the order of 1-2 μA . The BUF-03 has a lower maximum output current ($\pm 70mA$), but the advantage of an input current on the order of 200pA.

VARIOUS UNITY-GAIN BUFFERS,
THD + N (%) VERSUS FREQUENCY (Hz)
FOR $V_{out} = V_{in} = 10V$ rms, $R_L = 600\Omega$, $V_S = \pm 18V$

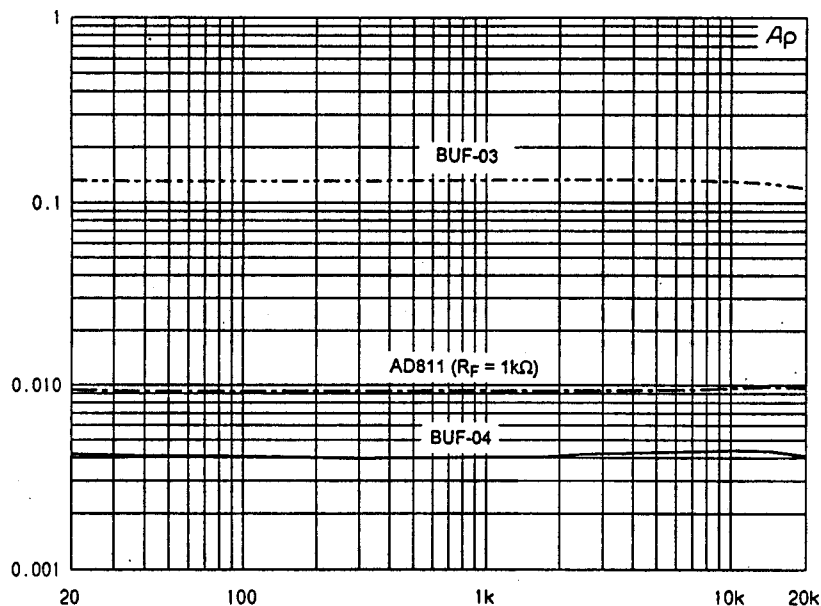


Figure 8.40

Capacitive Loading

Audio output/input stages are typically operated as voltage source drivers feeding high impedance loads. When connected with long transmission lines between stages, the result is that the driver sees an unterminated line, which can appear highly capacitive.

Audio driver stability with capacitive loading is not always easy to achieve.

Fortunately, some standard techniques exist for stabilizing op amp drivers with capacitive loads, and these can be implemented in a reasonably direct fashion.

A good rule for any type of audio driver is that capacitive loading should be expected in any application, however benign it may seem. Signal trace ca-

capacitance can build up quickly, even on the same PC board, and particularly for long signal runs. "Off board" circuits at the end of short cable runs should be evaluated for capacitive loading much more carefully, with the capacitive loading characterized as well as pos-

Overcompensation

Overcompensation of an op amp to achieve stability inadvisable with audio circuits, as it compromises both slew rate and bandwidth. Furthermore, few audio op amps provide the compensation pins to allow such overcompensa-

sible. "Outside world" drivers where load capacitance is either poorly defined or undefined must be considered a worst case, and bullet-proofed accordingly with appropriate design techniques.

tion (some exceptions to this are the 5534, the AD829, and the AD744). In some situations overcompensation may be useful, but generally other techniques for dealing with capacitive loads are more effective.

Passive Capacitive Load Compensation

A passive form of capacitive load compensation is the most simple and practical for general purpose audio circuits. Shown in Figure 8.41, this circuit stabilizes an amplifier output against capacitive load by isolating it with a series resistor, R_X . The amplifier feedback loop is *passively* buffered from capacitive load effects by R_X , and amplifier stability is maintained. The series resistor R_X does cause a voltage drop proportional to load current, so for low impedance loads it must necessarily be low. Typical R_X values will lie in the range of 10-50 Ω , which produce small but (usually) manageable power losses for loads of 500 Ω or more.

Obviously, the choice of U1 buffer amplifier must be consistent with the load requirements, and generally the ability to drive high currents is an

advantage. The AD845 is shown in this example, and is chosen for its minimum gain of 100kV/V driving 500 Ω or higher loads, output currents of up to ± 50 mA, and a slew rate of 100V/ μ s. In addition, it has a cascode FET input stage with low bias current, and low distortion.

For low impedance loads, R_X at 50 Ω produces a 10% gain error and a similar power loss. Gain accuracy also suffers, if the load is remote or its impedance is not known accurately.

If the load R_L is known and stable, then adding gain resistors R_F and R_{IN} can compensate for the gain loss caused by R_X . For this unity gain driver, when these resistors are matched in ratio to R_X/R_L , a nominal overall gain of 1 is restored.

PASSIVE CAPACITIVE LOAD ISOLATION USING ISOLATION RESISTOR, R_X

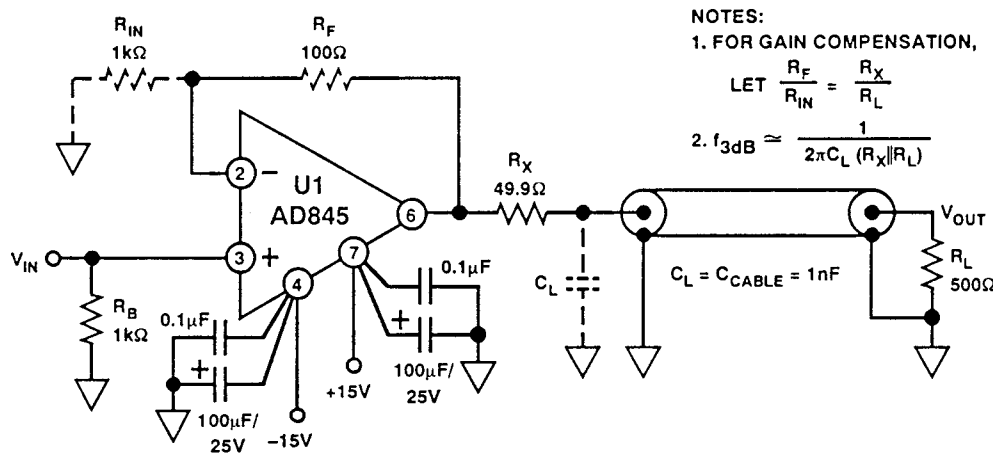


Figure 8.41

This capacitive load compensation technique is quite simple and can be effective, but it does have drawbacks. Already mentioned is loss of gain (or gain accuracy) and loss of output power, there is also loss of bandwidth for high values of load capacitance, and a possible loss of slew rate. For example, while the AD845 has a basic slew rate of 100V/μs, this falls to 50V/μs with $C_L=1nF$. In general the slew rate in this circuit will be limited to $I_o(max)/C_L$ V/s, when this figure is

smaller than the intrinsic device slew rate (as is the case here).

The technique of Figure 8.41 is a general one, and is useful with any amplifier. High speed, high current devices will of course make best use of it for audio. The applications following show op amps generally suited for line driving use by virtue of their unusually high current output, low output resistance, and/or speed capabilities.

Internal Capacitive Load Compensation

An even simpler method of driving capacitive loads is to use an op amp which has an *internal* load compensation network. This is an amplifier design feature that makes capacitive loading virtually transparent to the user. It is used in a number of ADI op amps, including the AD817, the AD829, and the AD847.

As the simplified AD817 schematic in Figure 8.42 shows, part of the amplifier compensation network is capacitor C_F , which is connected in a feedforward fashion around the unity gain output

stage. Under normal circuit operation with low capacitive loads this network is bootstrapped by the output stage, little voltage appears across it, and it has little effect on the output. With capacitive loading and large signals, current is drawn from the output stage, which causes a voltage drop across the C_F network and a corresponding current in it. This adds additional compensation capacitance to the amplifier's internal compensation node, slowing down the amplifier and keeping it stable.

AD817 SCHEMATIC ILLUSTRATING INTERNAL CAPACITIVE LOAD COMPENSATION

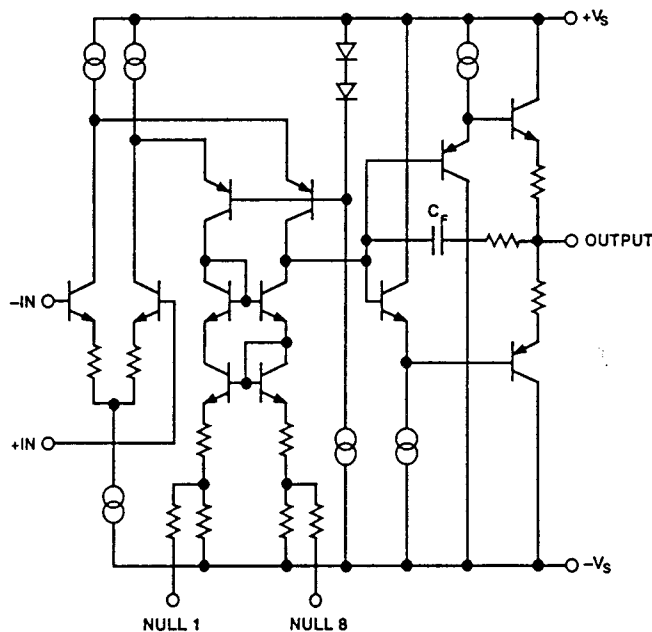


Figure 8.42

Like the passive form of capacitive load compensation, internal compensation causes in loss of bandwidth and slew rate. In addition it is signal dependent,

having greater effect with large signals than small ones. It can also cause some distortion, since the amplifier bandwidth varies dynamically.

External "In Loop" Capacitive Load Compensation

External *in loop* compensation is the most flexible and accurate of the compensation techniques available for capacitive load isolation. It is flexible because it can, in principle, be applied to any unity gain stable op amp, whether it is operating in inverting or non-inverting mode. It is accurate because it includes the isolation resistance R_X within a DC feedback loop. This feature makes the low frequency gain accuracy as good as the resistors used (assuming adequate gain in the op amp). Its main problem is that it re-

duces bandwidth and slew rate, like the other techniques we have discussed.

The basic circuit illustrating operation is shown in Figure 8.43. It is a non-inverting stage with a gain of 2, where resistor R_X isolates the capacitive load C_L . While the circuit is similar to that in Figure 8.41, the resistive feedback is taken from the *load* side of R_X , automatically compensating for gain errors and loading. The basic gain expression is similar to that of a standard non-inverting op amp stage.

8

CAPACITIVE LOAD ISOLATION USING "IN-LOOP" COMPENSATION

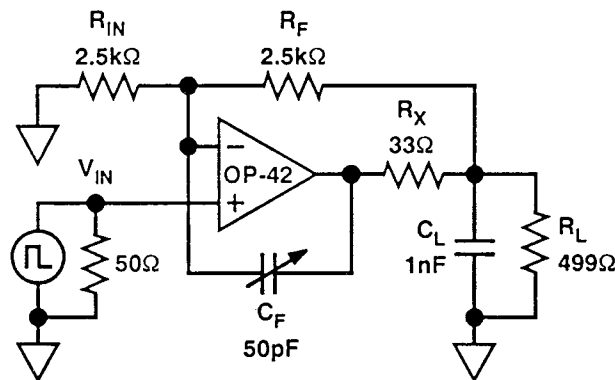


Figure 8.43

The capacitor C_F provides compensation for the additional lag introduced by C_L . C_F can be adjusted to cancel the effect of C_L and provide a well damped step response. This counters the ten-

dency towards overshoot, ringing or oscillation caused by C_L , but it does not allow maximum bandwidth, as the closed loop bandwidth of the stage is still a function of R_X and C_L .

The value chosen for R_X is not critical, and the stage can be tuned with values in the range of 10-100 Ω . R_X should not be excessively large, as this will degrade power output as well as bandwidth.

The optimum value for C_F is a function of R_X , C_L and the gain resistors, and with fixed values for R_F , R_{IN} and R_X , will track C_L . While several references suggest procedures for predicting C_F ,^[7,8] the best practical approach is to select a close nominal value for C_F ,

then adjust it for optimum pulse response *in the final circuit layout*.^[9] This approach takes additional parasitic capacitances into account.

Low values of R_F/R_{IN} minimize sensitivity to stray capacitance. This will force C_F higher than 20pF and into a range of greater predictability and stability. C_F is best a composite of an NPO capacitor in parallel with an NPO trimmer. Alternately, it can be a single fixed value, once the optimum value has been verified in final layout.

Op Amp Device/Topology Related Distortions

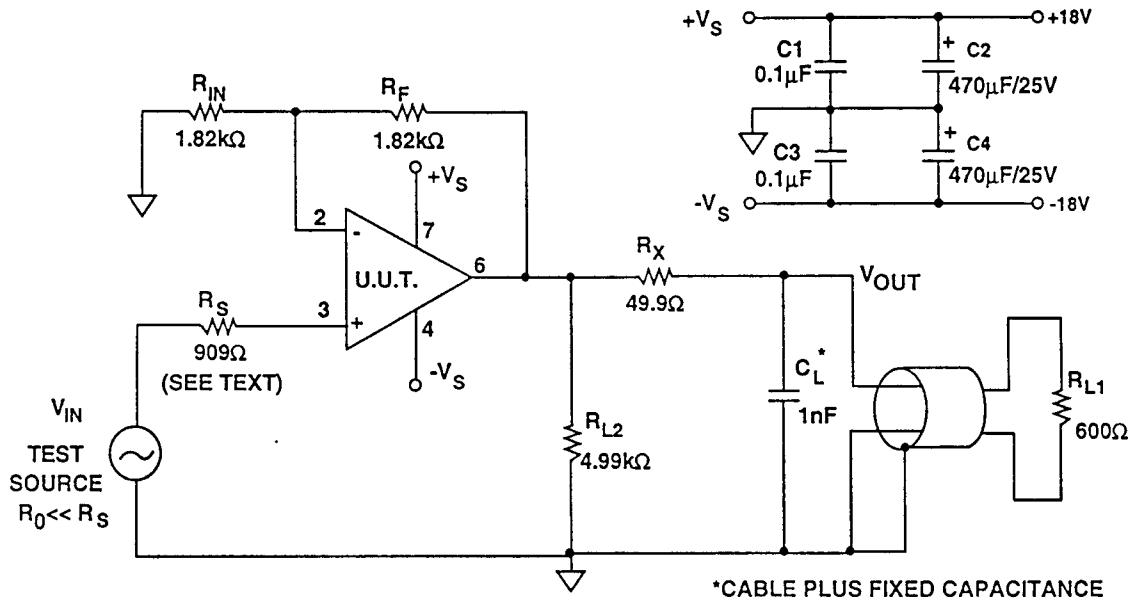
Single-ended audio drivers can be built using Figure 8.41 as a starting point, and that circuit, with appropriate choice of op amp and gain can well serve as a basic audio driver. The non-inverting gain stage architecture is preferable for a line driver, since it loads the signal source less, and it does not invert. However, this configuration is subject to certain distortions, which should be understood in order to obtain the best performance in an application.

The test circuit in Figure 8.44 loads the amplifier with 500 Ω and 1nF. Such a load is quite difficult to drive, so this test is useful for discovering the behavior of devices under adverse load conditions. By programming a gain of 2 the test ensures the presence of sufficient common-mode voltage to test for common-mode related distortion as well. The tests are conducted with $\pm 18V$

supplies and an analyzer bandwidth of 10 Hz-80kHz. We find that amplifiers with linear output stages and high drive capability may still exhibit non-linearity in this test, due to the non-linear C/V characteristics of the amplifier inputs. The effect can be minimized by matching the source impedances at +In and -In, which reduces the differential component of this error.

This point is illustrated by Figure 8.45, a family of plots for the OP-275 op amp tested in the circuit of Figure 8.44, using various values of source resistance R_S . Distortion is lowest when R_S is equal to the parallel equivalent of R_F and R_{IN} , (about 910 Ω). For higher or lower values of R_S , distortion rises. Appreciably higher source impedance (10k Ω) can cause the distortion to occur at lower frequencies, making performance much worse overall.

TEST CIRCUIT FOR LINE DRIVER AMPLIFIERS



8

Figure 8.44

FOLLOWER MODE R_S SENSITIVITY: OP-275
 THD + N (%) VERSUS FREQUENCY (Hz) FOR
 $V_{out} = 7V$ rms, $R_S = 910\Omega, 100\Omega, 10k\Omega, R_L = 500\Omega, V_S = \pm 18V$

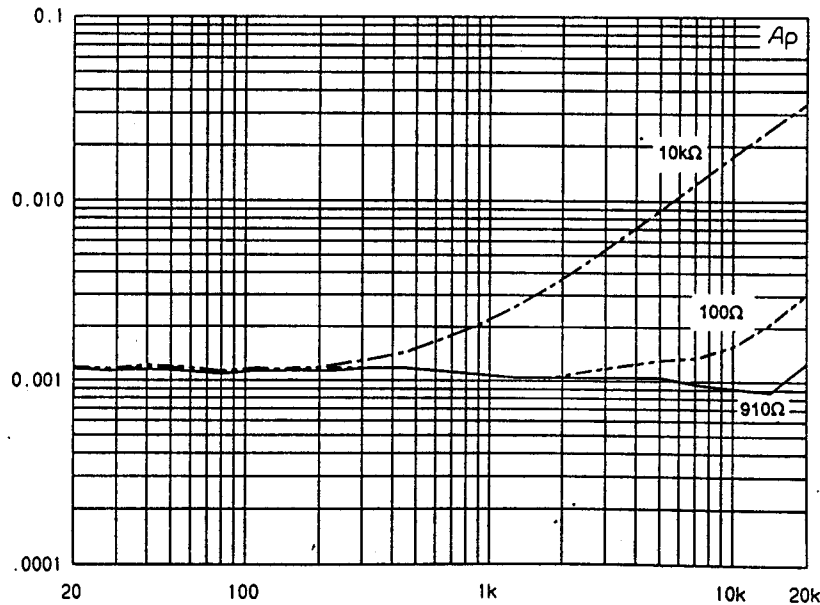


Figure 8.45

Whenever possible, amplifiers which operate as voltage followers should have their source impedances balanced for lowest distortion. The OP-275 device is but one example, and its sensitivity to CM distortion effects is not at all unique. Most solid-state amplifiers (op-amps, in-amps, and discrete bipolar transistors and FETs) are subject to nonlinear C/V effects to some extent. In the tests of other amplifiers, R_S was maintained at 910Ω to minimize the effects of this distortion mechanism.

With high output, high slew rate linear amplifiers, the distortion generated for

these test conditions can be comparable to the distortion of the test equipment (Figure 8.46). Here the AD817, AD818 and AD845 amplifiers show THD+N which is essentially equal to the residual distortion of the measurement system for these conditions, and appreciably below 0.001%.

Amplifier types expressly designed for audio use do well in these THD+N tests, (Figure 8.47). The industry standard 5534 is near or just above the residual level, the OP-275 plot falls just above 0.001%, and the 5532 is slightly higher.

SET "A" DRIVERS, THD + N (%) VERSUS FREQUENCY (Hz)
 FOR $V_{out} = 7V$ rms, $R_S = 909\Omega$, $R_L = 500\Omega$, $V_S = \pm 18V$

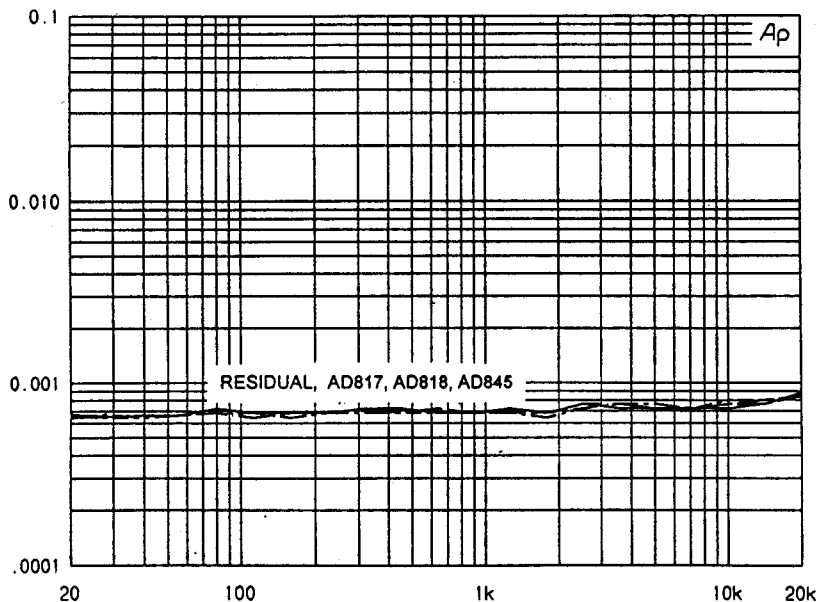


Figure 8.46

SET "B" DRIVERS THD + N (%) VERSUS FREQUENCY (Hz)
 FOR $V_{out} = 7V_{rms}$, $R_S = 909\Omega$, $R_L = 500\Omega$, $V_S = \pm 18V$

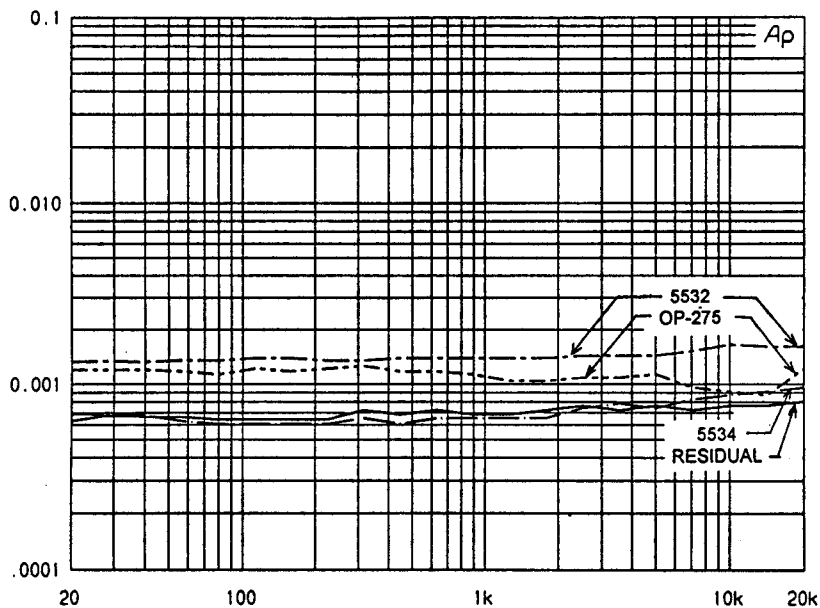


Figure 8.47

8

SINGLE-ENDED LINE DRIVERS

This section discusses a variety of line drivers which drive single-ended lines,

optimized for different environments.

Consumer Equipment Line Driver

One common driver application is a line output stage for consumer preamps, CD players, etc. This is an economical stage with a nominal gain of 5 to 10 times operating from supplies of $\pm 10V$ to $\pm 18V$, with a rated output of 2-3V_{rms} driving loads of 10k Ω or more. For

simplicity of biasing and minimum output DC offset, AC coupling is used, and the circuit is often fed from a volume control. Such a stage is shown in Figure 8.48, using an OP-275 op amp as the gain element.

CONSUMER EQUIPMENT LINE DRIVER

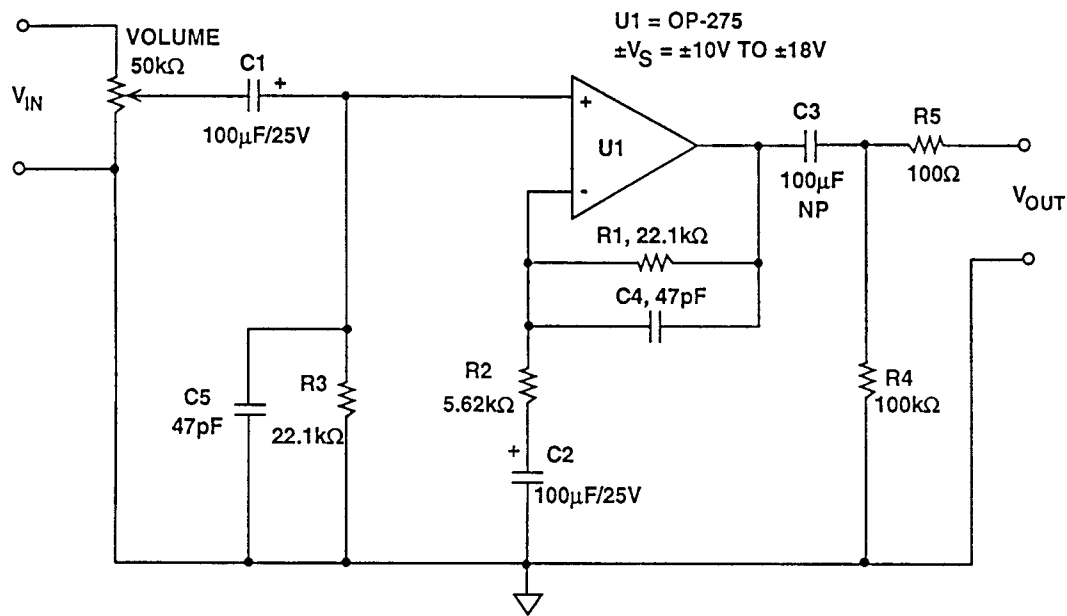


Figure 8.48

In this circuit input and feedback resistors R_1 and R_3 are made equal, so the nominal DC bias at $U1$'s output is zero. The $U1$ bias current flowing in these resistors polarizes coupling capacitors C_1 and C_2 . The OP-275 has PNP input transistors, so this bias is positive. If the OP-275 is replaced with an amplifier with NPN input transistors, the polarity will be reversed and the polarity of C_1 and C_2 should also be reversed. R_1 and R_2 set the stage gain (nominally 5). R_2 and C_2 set the LF rolloff at 0.3 Hz. This allows the gain to be increased by reducing R_2 without changing C_2 . The output capacitor, C_3 , must be non-polar, since the output offset may be of either polarity. If the

output can tolerate a DC offset of ± 10 mV (max - typical value is ± 2.5 mV), C_3 may be omitted.

THD+N performance of the stage is shown in Figure 8.49 for outputs of 1, 2, and 3V_{rms} into a 10k Ω /600pF load, using ± 18 V supplies with an R_S of 1k Ω . At lower output levels performance is noise limited, while at a 3V output level there is a slight increase in high frequency distortion. Although this application is an example of a circuit where the amplifier source impedances cannot be perfectly matched (due to variations of the volume control), performance is still good.

**CONSUMER EQUIPMENT LINE DRIVER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR $V_{out} = 1, 2, 3V$ rms, $R_L = 10k\Omega/600pF$, $V_S = \pm 18V$**

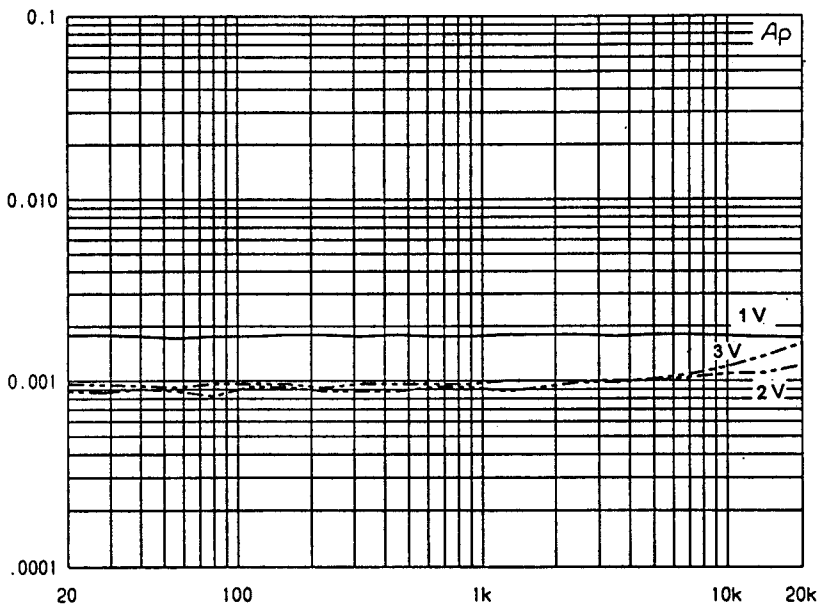


Figure 8.49

Noise is the limiting factor for lower level signals, and if lower noise is required, R_2 can be reduced. The practical limit to noise is the volume control's finite output resistance which causes higher noise at high output resistance, because of interaction with the noise current from U1. If the effective R_S at the volume control is $10k\Omega$, a $1.2pA/\sqrt{Hz}$ noise current from U1 will

produce an input referred $12nV/\sqrt{Hz}$ noise voltage.

The driver stage of Figure 8.48 is flexible, and also operates at supplies as low as $\pm 10V$ with outputs up to $3V_{rms}$, with a slight distortion increase. At $\pm 5V$, outputs up to $2V_{rms}$ are possible, but with distortion still higher but remaining $\leq 0.01\%$.

Paralleled Output Line Driver

Often a modest increase in output may be needed from a driver, but circumstances may not warrant the use of an additional buffer. Figure 8.50 shows how the second section of a dual op amp can be used to provide additional load drive. In this circuit, the U1A section is an $\times 5$ voltage amplifier, while U1B is a voltage follower, used simply to provide

additional current to the load. Current sharing between the amplifier stages is determined by output resistors R_4 and R_5 , and the composite stage drives 600Ω loads with lower distortion than a single OP-275 section. THD+N data is shown in Figure 8.51 operating from $\pm 18V$ supplies, and for output levels of 1, 2, 5, and $9V_{rms}$ into 600Ω .

PARALLELED OUTPUT LINE DRIVER

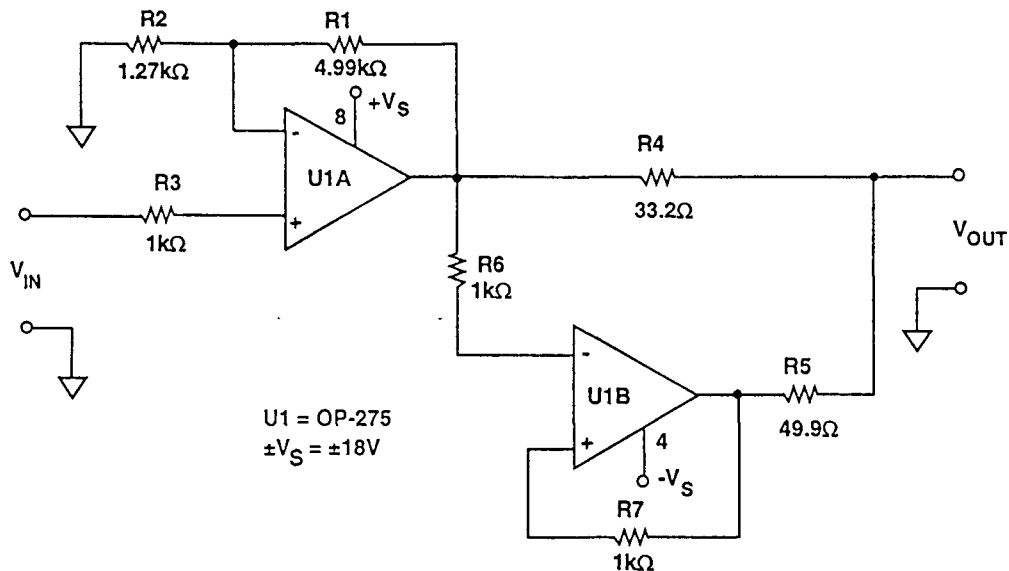


Figure 8.50

PARALLELED OUTPUT LINE DRIVER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR V_{out} = 1, 2, 5, 9V rms, R_L = 600Ω, V_S = ±18V

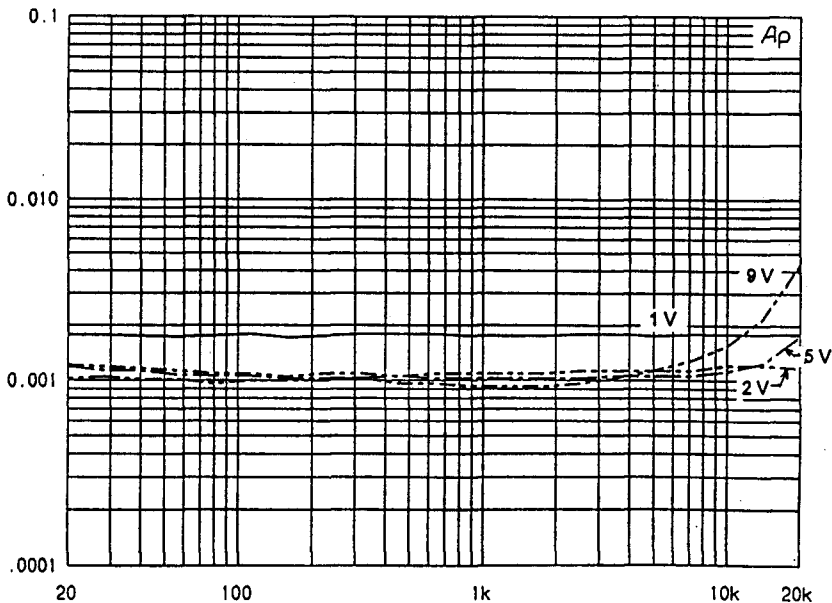


Figure 8.51

This scheme can be used with any unity gain stable dual op amp and various gain levels. For different devices and

gains the ratio of R_4 and R_5 may need adjustment for lowest distortion into the load.

A WIDE DYNAMIC RANGE ULTRA LOW DISTORTION DRIVER

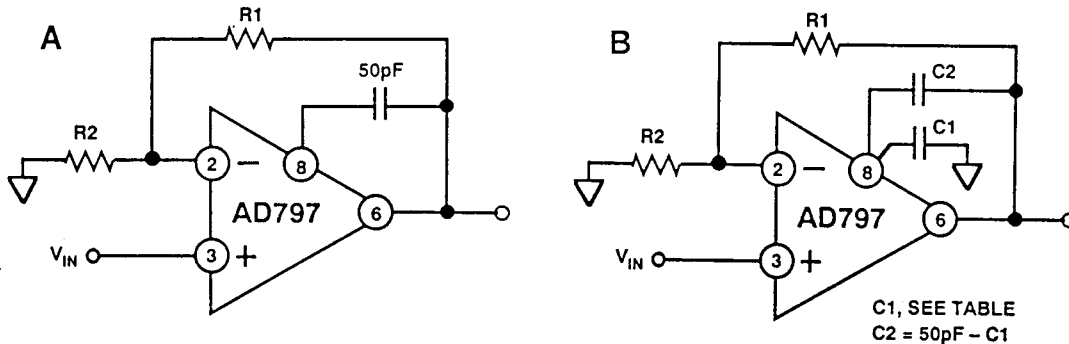
Single-ended line drivers may seem simple, but when both high dynamic range and low noise and distortion are necessary, it is difficult to choose a suitable amplifier.

allows improvements in bandwidth, phase margin, settling time, and noise over more conventional two-stage op-amps.

The AD797 has very low input noise of $<1 \text{ nV}/\sqrt{\text{Hz}}$ and a distortion cancelling output stage, and is exceptionally well-suited to line driver applications.^[11]

The AD797 is used like any other 5 pin op amp (Figure 8.52). Low values for gain resistors R_1 - R_2 are recommended for best noise, and selecting these resistors should be done with care, as values $\geq 100\Omega$ will limit noise performance. Suggested values for gains of 10-1000 times are noted in the "A/B" column of the table in Figure 8.52. The AD797 can drive loads of up to 50mA, and is specified for distortion when driving loads of 600Ω .

AD797 RECOMMENDED CONNECTIONS FOR DISTORTION CANCELLATION AND BANDWIDTH ENHANCEMENT



	A / B		A			B		
	R1 Ω	R2 Ω	C1 pF	C2 pF	3dB BW	C1 pF	C2 pF	3dB BW
G=10	909	100	0	50	6 MHz	0	50	6 MHz
G=100	1k	10	0	50	1 MHz	15	33	1.5 MHz
G=1000	10k	10	0	50	110 kHz	33	15	450 kHz

Figure 8.52

For amplifier applications requiring the best possible distortion, the capacitors C_1 and C_2 should be used. The single 50 pF capacitor, C_2 , in Figure 8.52A compensates for output stage distortion without affecting forward gain.

At higher gains a second capacitor, C_1 , from the compensation node to ground, enhances open-loop bandwidth and improves high frequency performance by "decompensating" the amplifier and increasing its gain-bandwidth product (Figure 8.52B). The effects of C_2 , and C_1 and C_2 , are summarized in the table.

A family of distortion curves for various AD797 gain configurations driving 600Ω is shown in Figure 8.53. At low frequencies the noise is far greater than the distortion, which cannot be measured. At high frequencies distortion is measurable, but still extremely low. The distortion for a gain of 10 times at 20kHz for example, is $\approx 0.0001\%$, implying a dynamic range of 120dB referenced to $3V_{rms}$, and even more at higher level signals.

TOTAL HARMONIC DISTORTION (THD) VERSUS FREQUENCY @ 3V rms FOR AD797 DISTORTION CANCELLATION AND BANDWIDTH ENHANCEMENT CIRCUIT

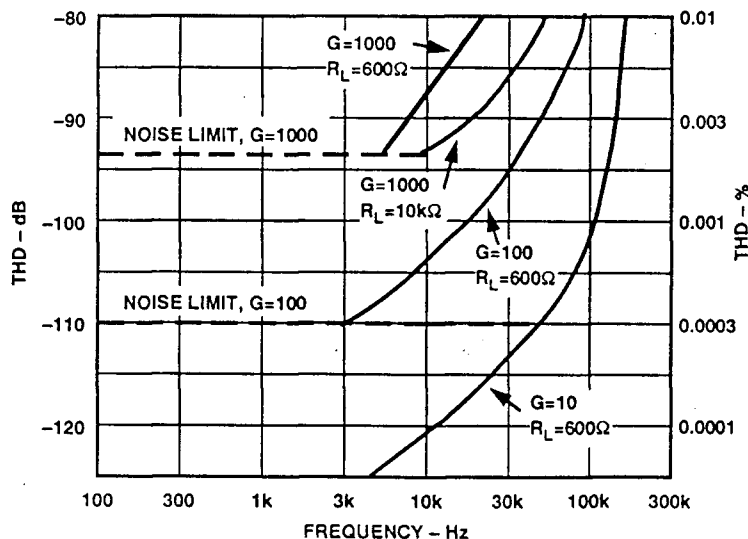


Figure 8.53

Current Boosted Line Drivers

When a driver must drive loads of less than $600\ \Omega$, it is unlikely that an op-amp can handle the task unaided. In such cases a current-boosted design allows loads down to $150\ \Omega$.

Figure 8.54 is an example of a high quality current boosted driver. It uses an AD845 as a gain stage and voltage driver, and a unity gain current booster. The overall voltage gain is $\times 5$, but may easily be modified by R_1/R_2 . For lowest CM distortion, R_3 is set equal to $R_1 \parallel R_2$.

The amplifier used for U2 may be either the AD811 op amp, or the BUF-04 buffer. The AD811 op amp is configured as a follower, with R_5 connected as shown. The BUF-04 is internally con-

nected as a follower. In either case, both the U1 and U2 devices *must* have a heat sink, and be used with supplies of $\pm 17\text{V}$ or less. As usual, the power supplies must be well bypassed.

For loads of $150\ \Omega$, the series isolation resistor R_4 is only to $22.1\ \Omega$, to minimize power loss and to allow levels of 7V_{rms} or more. The THD+N data for this circuit is shown in Figure 8.55 and Figure 8.56 respectively, using the AD811 and BUF-04 as the U2 buffer. The test conditions are successive input sweeps resulting in 1, 2, 4 and 8V_{rms} out. The test power supplies are exactly $\pm 18\ \text{V}$. *Production versions of this circuit, where the power supplies will be less accurately defined, should use nominal supplies no greater than $\pm 17\ \text{V}$.*

8

CURRENT BOOSTED LINE DRIVER

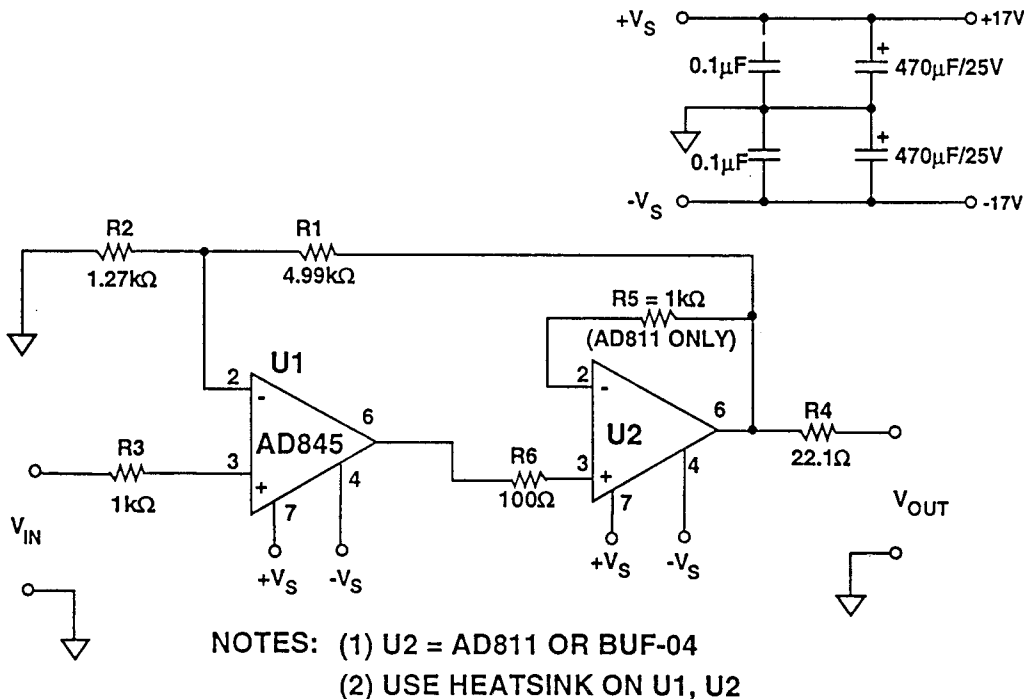


Figure 8.54

**CURRENT BOOSTED DRIVER USING AD811
 THD + N (%) VERSUS FREQUENCY (Hz)
 FOR $V_{out} = 1, 2, 4, 8V$ rms, $R_L = 150\Omega$, $V_S = \pm 18V$**

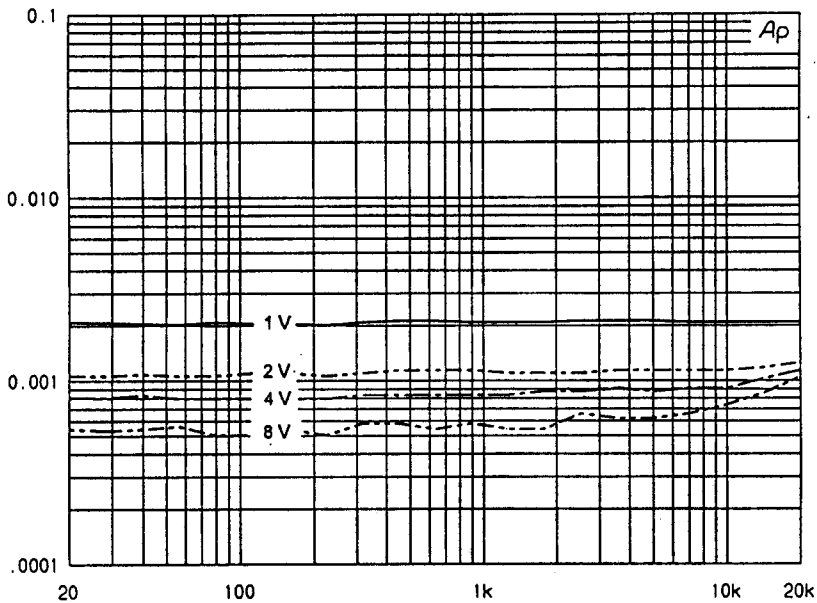


Figure 8.55

**CURRENT BOOSTED DRIVER USING BUF-04
 THD + N (%) VERSUS FREQUENCY (Hz)
 FOR $V_{out} = 1, 2, 4, 8V$ rms, $R_L = 150\Omega$, $V_S = \pm 18V$**

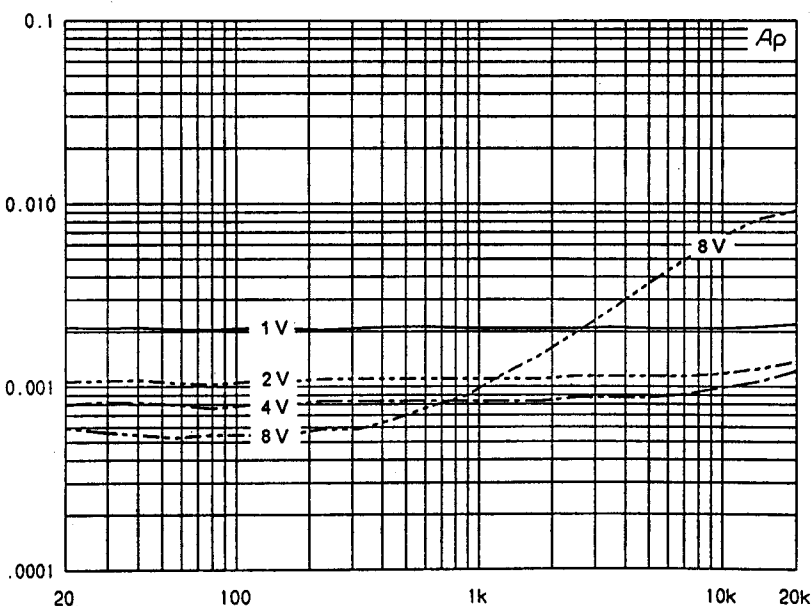


Figure 8.56

For the AD811 buffer, the data of Figure 8.55 shows THD+N dominated by noise and residual distortion at nearly all levels and frequencies while driving 150Ω . A very slight rise in distortion is noted above 10kHz, yet it is still $\approx 0.001\%$. The BUF-04 (Figure 8.56) is nearly as good at low output levels, but shows some distortion increase at the 8Vrms output at higher frequencies.

There is a tradeoff involved in the choice between these two devices. The

BUF-04 has a standby dissipation of about 300mW, while the AD811 has nearly double this dissipation, 560mW. So while the AD811 yields lower distortion, it must be operated more conservatively. Only the minimum supply voltage required to sustain a given output should be used.

Variants of this circuit technique will be found in later parts of this section in other driver applications.

A Composite Current Boosted Driver

Another useful current-boosted circuit technique combines the best features of two different amplifiers into a single composite structure, producing a very high performance line driver.^[12,13] With an FET input IC as the input stage, there is no noticeable dc offset change from source resistance variations of a typical volume control, allowing dc coupling. A high current, wide band current booster output stage drives line impedances down to 150Ω with excellent linearity.

A composite amplifier allows the best features of two dissimilar ICs to be exploited. Figure 8.57 shows a low distortion composite amplifier using two amplifier ICs.

A factor which aids performance is that U1 operates unloaded, and the compensation pin (5) drives U2. This removes possible U1 output stage distortion. The overall gain bandwidth and slew rate of U1 are boosted by the voltage gain of

U2, an AD811. The AD811 is used for its $\pm 150\text{mA}$ (max) output current.

The circuit has an overall gain of 5, set by R_1 and R_2 . The gain of the output stage, which is set by R_3 and R_4 , should be

$$\left[\frac{\text{Overall Gain} - 1}{2} \right]$$

As the AD811 is a transimpedance amplifier, there is an optimum value for R_3 , which should be used, and the gain varied with R_4 . Further design details are available in Reference 12.

The composite amplifier performance is remarkable for its modest complexity. For a typical audio load of 600Ω , THD+N at output levels of 1, 2, 4 and 8Vrms is shown in Figure 8.58. Distortion is only visible above the noise at the higher frequencies. The circuit will drive low impedance loads down to 150Ω . At supply voltages above $\pm 12\text{V}$, U2 requires a heat sink.

COMPOSITE CURRENT BOOSTED LINE AMPLIFIER

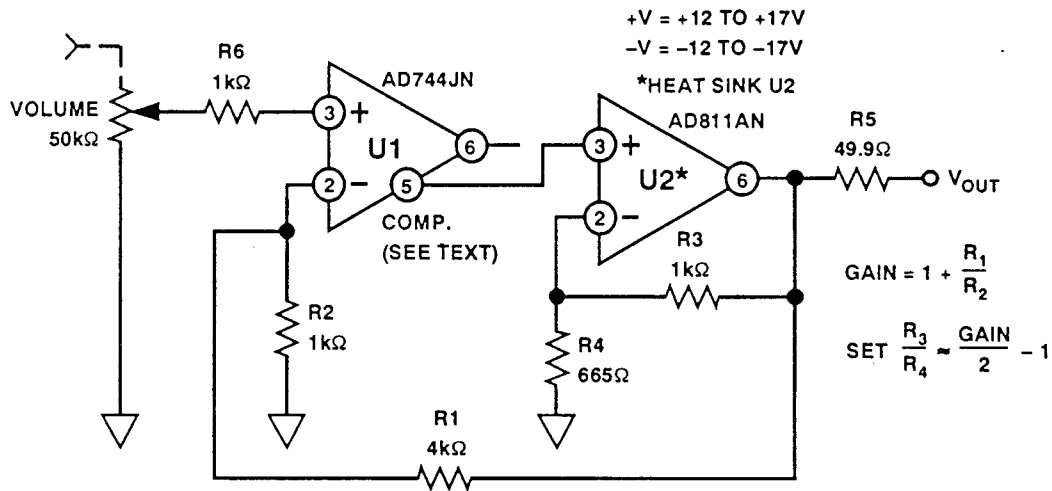


Figure 8.57

COMPOSITE CURRENT BOOSTED DRIVER THD + N (%) VERSUS FREQUENCY (Hz) FOR $V_{out} = 1, 2, 4, 8V$ rms, $R_L = 600\Omega$, $V_S = \pm 18V$

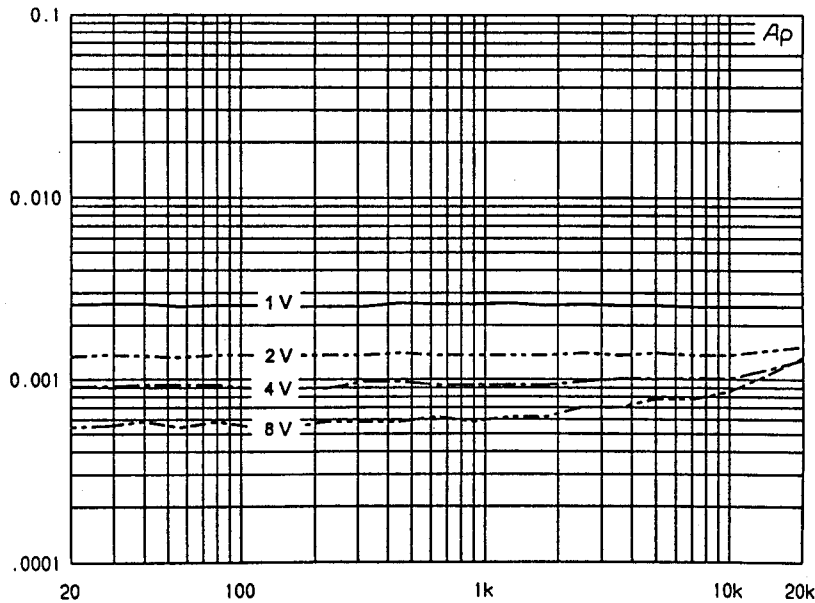


Figure 8.58

Differential Line Drivers

Standard circuits for line drivers are not nearly as well-defined as standard circuits for line receivers. This section

discusses a variety of possible circuits, varying greatly in complexity and performance.

“Inverter-Follower” Differential Line Driver

A straightforward approach to developing a differential drive signal of $2V_{IN}$ is to amplify in complementary fashion a single-ended input V_{IN} , with equal gain inverter/follower op amps. With op amp gains of ± 1 , this develops outputs $-V_{IN}$ and $+V_{IN}$ with respect to common, or $V_{OUT} = 2V_{IN}$ differentially. V_{OUT} can be scaled further, but gains $< \pm 1$ are less practical.

OP-275 and one $8 \times 20k$ film resistor network (Figure 8.59). Here U1A provides the gain of -1 , while U1B operates at a gain of $+1$. The differential output signal across the balanced output line is $2V_{IN}$, and the differential output impedance is equal to $R_A + R_B$, or 100Ω .

This “inverter/follower” driver is easily built with a dual op amp such as the

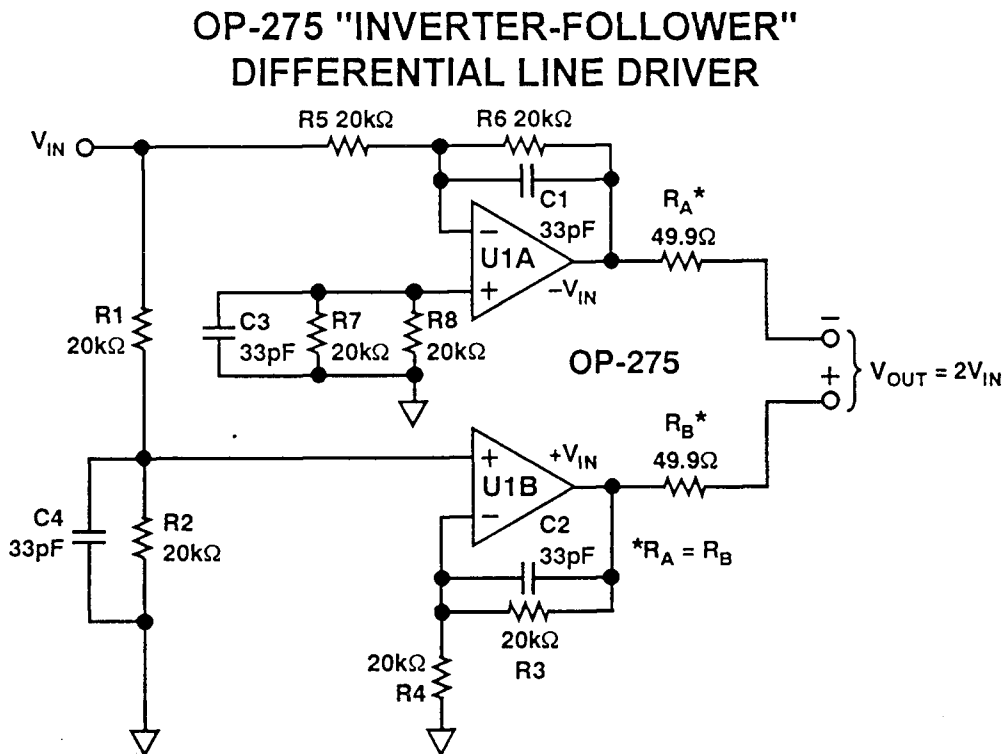


Figure 8.59

Use of similar values for gain resistors around the two amplifiers matches the channel noise gains, and makes the network easy to obtain. It also matches the source impedances seen by the op amp inputs. Capacitors C_1 - C_2 provide HF rolloff, and enhance stability when driving capacitive lines. This circuit has high performance for its cost and simplicity. If a resistor network is used for

R_1 - R_7 , it can be built with only 6 components.

THD+N performance of this circuit is shown in Figure 8.60. The distortion is about 0.001%, and somewhat higher at 1V output level (noise limited). Maximum output level is about 12Vrms into 600Ω before clipping.

OP-275 "INVERTER-FOLLOWER" DIFFERENTIAL DRIVER
 THD + N (%) VERSUS FREQUENCY (Hz)
 FOR $V_{out} = 1, 2, 5, 10V$ rms, $R_L = 600\Omega$, $V_S = \pm 18V$

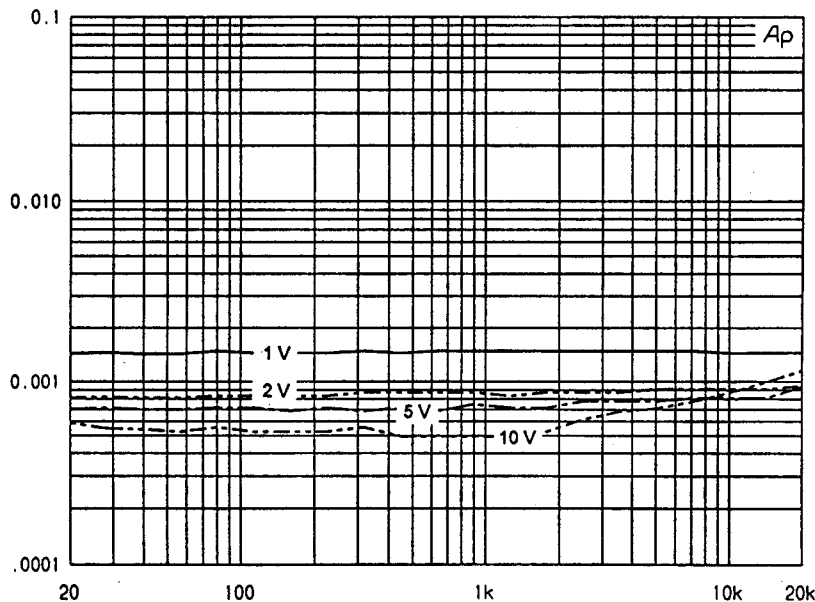


Figure 8.60

This type of differential line driver can run into application problems, and should be used with some care. The driver circuit uses two single-ended drivers, and they produce output signals with respect to the source (V_{IN}) common point.

If the receiver used with this driver has a high impedance differential input (such as those discussed in the line receiver section) there is no real problem. However, one side of the differential output from Figure 8.59 *cannot be grounded without side effect*. This is

because the source drive V_{OUT} is *not* floating.

In this sense, the circuit is *pseudo differential*, and it should not be used indiscriminately. Nevertheless, within small and well defined systems, it has

the obvious advantage of simplicity and can achieve high performance. With the matched sources R_A and R_B of 49.9Ω there will be no damage even if one output is shorted, but half the signal will be lost.

Cross-Coupled Differential Line Driver

A more sophisticated form of differential line driver uses a pair of *cross-coupled* op amps with both positive and negative feedback paths. The general form of this type of circuit is a cross-coupled *Howland* circuit, named after the inventor of the classic resistor bridge current pump. The cross-coupled form was described by Pontis in a solid-state transformer emulator for high performance instrumentation.^[14]

signal V_{OUT} to be maintained independent of the load common connections. This means that either side can be shorted to common, as with a transformer.

This configuration provides maximum flexibility, allowing a differential output

Figure 8.61 shows the SSM-2142 balanced line driver IC use. The SSM-2142 consists of two cross-coupled Howland circuits, plus an input buffer. The trimmed multiple resistor array and three op amps are packaged in an 8 pin miniDIP IC.

8

SSM-2142 CROSS-COUPLED DIFFERENTIAL LINE DRIVER USED IN BALANCED DRIVER / RECEIVER SYSTEM

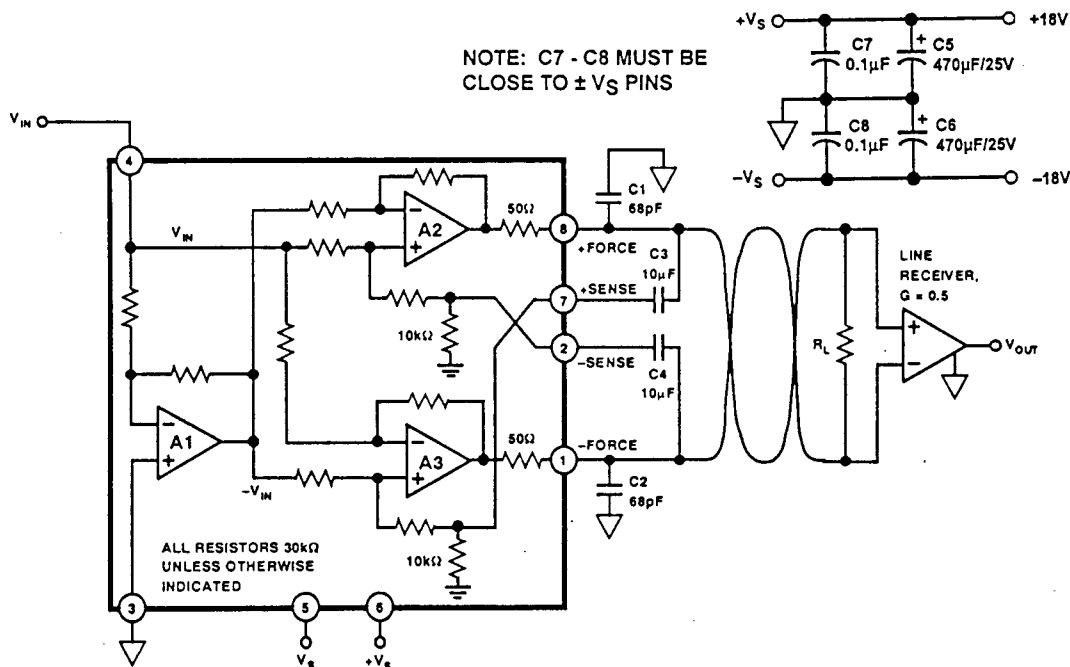


Figure 8.61

The SSM-2142 line driver is designed for a single-ended to differential gain of 2 and will drive a 600Ω load. In the simplest use, it is simply strapped with the respective output FORCE/SENSE pins tied together (7-8, 1-2). Small film capacitors C_1 - C_2 preload the IC for stability against varying cable lengths. To decouple line dc offsets, the optional capacitors C_3 - C_4 are used, which should be non-polar types, preferably films. The $0.1\mu\text{F}$ low inductance bypass caps C_7 & C_8 must be within 0.25" of power supply pins 5 and 6 as long lead lengths will cause excessive THD.

In a system application, the SSM-2142 is used with a gain of 0.5 receiver,

either an SSM-2143, or one of the other line receivers discussed previously. The system shown in Figure 8.61 comprises an entire single-ended to differential and back to single-ended transmission system, with noise isolation, and net unity gain.

Figure 8.62 shows the THD+N performance of the SSM-2142 driver portion of Figure 8.61. Performance is noise limited for the 1V output curve, and distortion drops to $\leq 0.001\%$ for higher levels, rising with higher frequencies and at 10V output.

**SSM-2142 CROSS-COUPLED DIFFERENTIAL DRIVER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR $V_{out} = 1, 2, 5, 10\text{V rms}$, $R_L = 600\Omega$, $V_S = \pm 18\text{V}$**

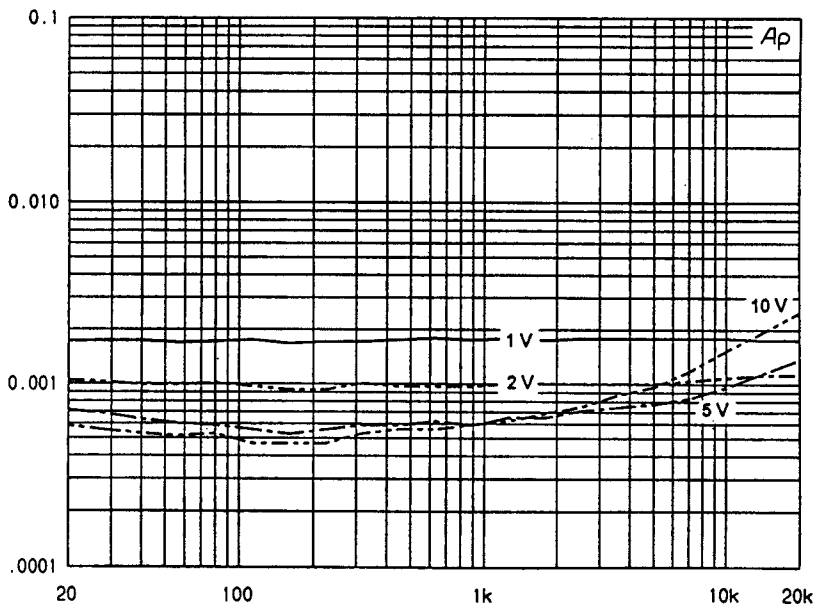


Figure 8.62

Transformer Coupled Line Driver

Transformers provide a unique method of signal coupling, which allows complete common-mode isolation. As noted in the section on line receivers, transformers are not without their technical and practical limitations, but their singular ability to galvanically isolate grounds maintains a place for them in difficult applications.^[15,16]

The circuit of Figure 8.63 is a low DC offset, high linearity driver circuit using a high quality nickel core output transformer. U1 and U2 form a high current driver, similar to the current boosted driver of Figure 8.54.

In this circuit U1 is selected as a low bias current, low offset voltage FET

input op amp, in order to hold the DC offset at the primary of T1 to a minimum (less than $\pm 15\text{mV}$). The DC current flowing into the primary winding of a transformer should be minimized, in order to minimize distortion. At the input to U1, C₁ (a high quality film capacitor) decouples any DC offset present on the signal input V_{IN}.

The U1-U2 device combination is capable of providing $\pm 100\text{mA}$ or more, which allows this circuit to drive low impedances. Although T1 is shown with a 1:1 ratio, other winding configurations are possible, allowing the circuit to drive a wide range of load resistances.

TRANSFORMER COUPLED LINE DRIVER

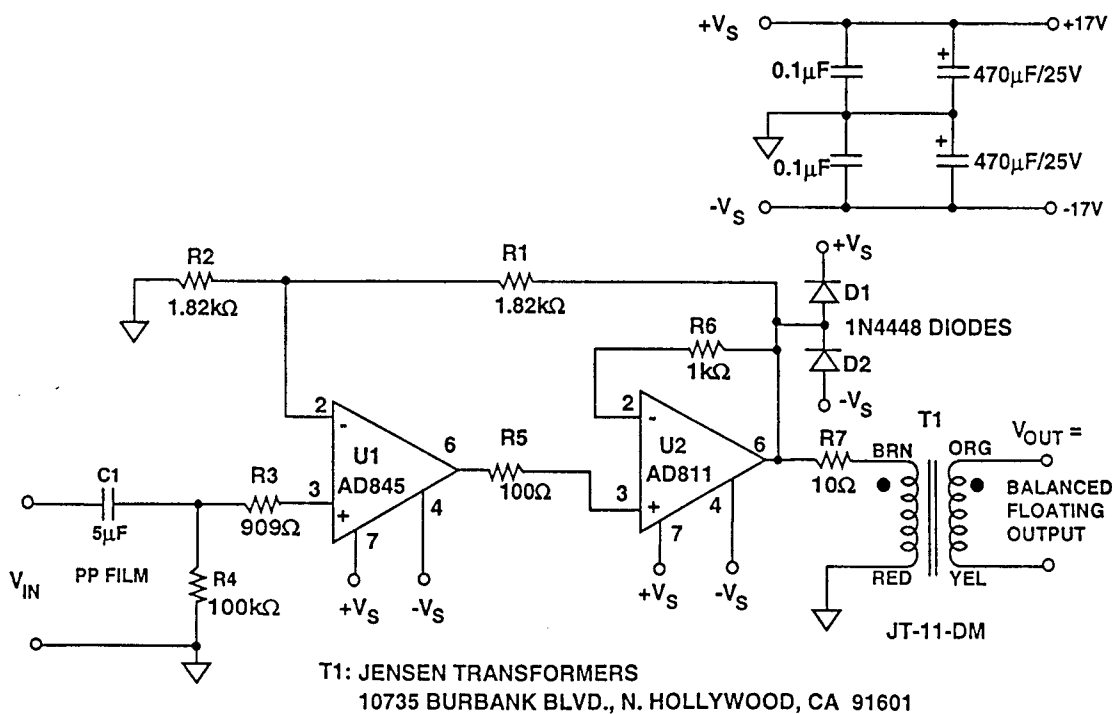


Figure 8.63

**TRANSFORMER COUPLED DRIVER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR $V_{out} = 1, 2, 4, 8V$ rms, $R_L = 600\Omega$, $V_S = \pm 18V$**

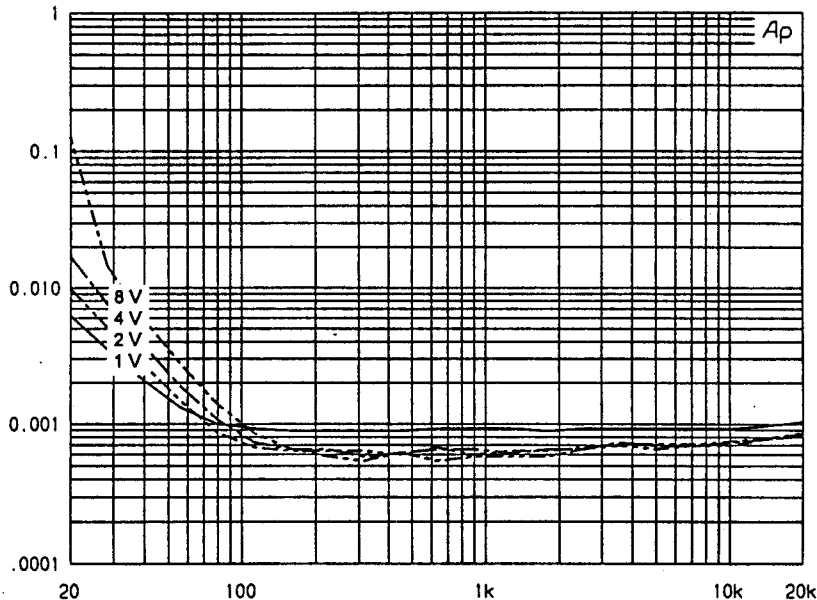


Figure 8.64

THD+N performance for this driver-transformer combination is shown in Figure 8.64. Like the 2x or 5x basic drivers previously described, its performance is essentially distortion free

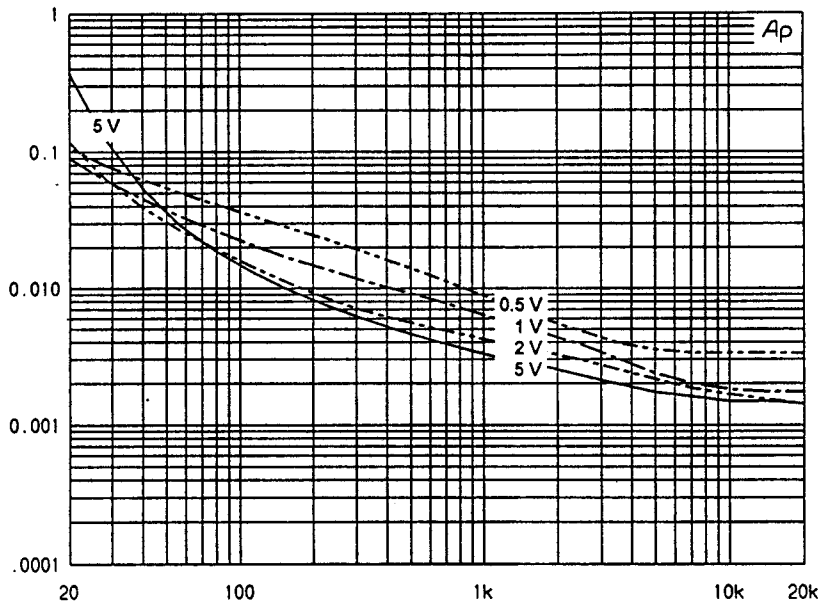
above 100Hz. At lower frequencies there is seen a level and frequency dependent distortion rise which reaches a maximum at 20Hz with output levels of 8Vrms (20dBm).

Transformer Coupled Line Driver with Feedback

Steel core transformers are more economical than nickel core ones, but have higher distortion. To further complicate design, the nonlinear distortion characteristics of steel core transformers vary with level and frequency in a complex way, rising at low levels and low frequencies. Their behavior is less forgiv-

ing than that of the nickel core types, and complicates their use in audio drivers. A family of distortion curves for a typical steel core transformer illustrates this behavior, shown in Figure 8.65. This series of curves is for a Jensen JT-123-S transformer.

**STEEL CORE TRANSFORMER
THD + N (%) VERSUS FREQUENCY (Hz)
FOR $V_{out} = 5, 2, 1, 0.5V$ rms, $R_L = 600\Omega$**



8

Figure 8.65

**TRANSFORMER COUPLED LINE DRIVER
WITH TERTIARY FEEDBACK**

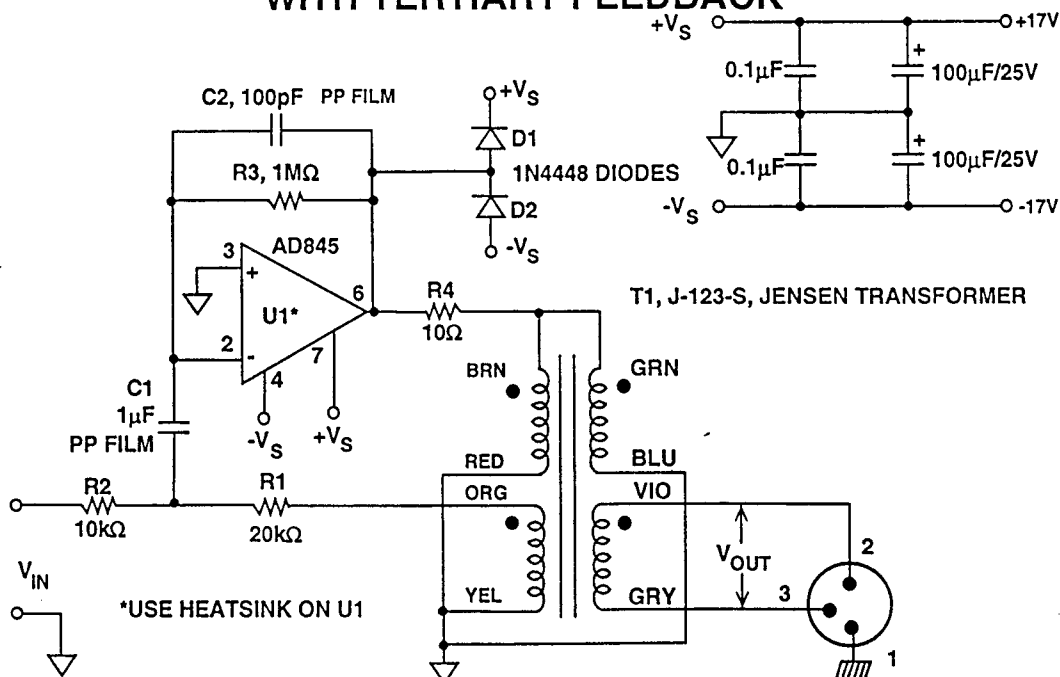


Figure 8.66

If a steel core transformer has several tightly-coupled windings, one may be used in a feedback loop to minimize the effects of the transformer non-linearity.

The circuit of Figure 8.66 is a low distortion driver using the quad-filar wound JT-123-S transformer, and an AD845 as the amplifier. Two parallel windings are used as the primary, feedback is taken from one secondary, and another drives the balanced 600Ω load.

To minimize DC offset, an FET input op amp is used, with local DC feedback via R_3 . This ensures that the maximum DC at the primary is no more than the sum of the amplifier V_{os} and $I_{bias} \times R_3$. For bias currents greater than 1nA and a high value for R_3 , the bias current component may become the dominant DC error. As a consequence a FET input device should be used for U1. Since the AD845 can also dissipate $\geq 300\text{mW}$, a heat sink will minimize temperature and hence bias current.

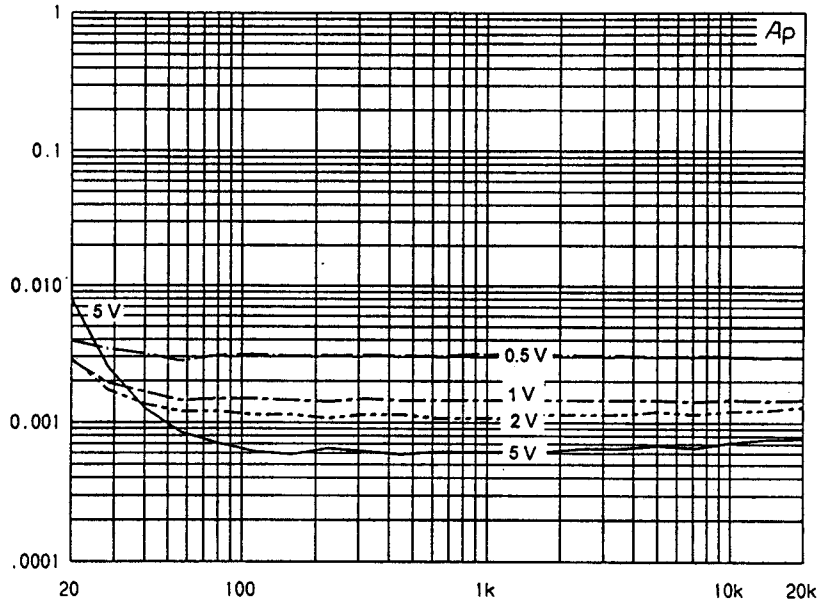
The transformer feedback loop is closed via R_1 , R_2 and C_1 , which cause the overall U1-T1 combination to act as an inverting amplifier for audio signals. As with a standard inverting amplifier,

gain is set via R_1 and R_2 , which in this case provide an (unloaded) gain of 2x from V_{IN} to V_{OUT} . High quality film capacitors are recommended for C_1 and C_2 , but their exact values and tolerances are not critical.

THD+N performance of this feedback driver is shown in Figure 8.67 using the specified JT-123-S transformer. A comparison of these data with those of Figure 8.65 demonstrates the effectiveness of the distortion reduction, and the variation of distortion with level and frequency. At some points the improvement is more than an order of magnitude.

Some precautions are necessary for the effective use of this circuit; they are mostly concerned with circuit dynamics. The circuit should not be overdriven, particularly at low frequencies, as the resulting distortion can be quite high. Clamping diodes D1 and D2 absorb any inductive kicks from T1 which might damage U1. The output of the basic circuit is limited to just over $5V_{rms}$ into 600Ω at low frequencies, but this can be increased by using a buffered driver for U1 (similar to that in Figure 8.63), and a larger transformer for T1.

STEEL CORE TRANSFORMER WITH FEEDBACK DRIVER
 THD + N (%) VERSUS FREQUENCY (Hz)
 FOR $V_{out} = 5, 2, 1, 0.5V$ rms, $R_L = 600\Omega$, $V_S = \pm 17V$



8

Figure 8.67

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APPENDIX: DC SERVO CONTROLLED AUDIO STAGES

With multiple stages of audio-frequency gain, the accumulation of DC offsets in various amplifiers can lead to problems. A classical solution to decoupling DC offset has been to employ input/output coupling capacitors. Typically, this involves the use of large value electrolytic capacitors (100 to 1000 μF) when operating into low impedances.

Modern low-bias-current, low-offset-voltage op amps allow simple elimination of coupling capacitors in many instances. For example, the use of low bias current, low offset voltage FET

input amplifiers such as AD711/AD712/AD713, AD744/AD746, and OP-249 in a basic gain-of-10 stage will not generally require capacitive coupling. With an appropriate device choice, output offset can be held to as low as $\pm 10\text{mV}$ or less, and will scarcely vary with source resistance.

This is one approach to the elimination of coupling capacitors. A more general approach which has come into vogue in recent years is the use of a *DC servo amplifier* stage, for output offset elimination.

8

NON INVERTING GAIN STAGE WITH SERVO

The circuit of Figure 8.68 is a standard non inverting audio voltage-amplifier gain stage (U1), with a non inverting integrator feedback stage connected around it (U2). For normal audio input signals, the gain of this stage is defined conventionally; that is, it is the ratio of the U1 feedback resistance (R_2) to the total resistance from the inverting input to ground plus 1. In this instance, the resistance to ground is made up of the parallel equivalent resistances of R_3 and R_4 , so the net gain " $G_{(U1)}$ " of stage U1 is:

$$G_{(U1)} = 1 + \frac{R_2}{R_3 \parallel R_4} \quad \text{Eq. 8.23}$$

In the servo circuit R_5 - C_1 and R_6 - C_2 form the integration time constants, which should be well matched in this form of integrator. The DC feedback from stage U2 is applied to the inverting input of U1 via R_4 . The servo loop forces the net DC output of amplifier stage U1 to a very low level. In practice, the DC output offset of U1 becomes equal to the offset voltage of amplifier U2.

Two factors affect the low frequency rolloff of the U1 gain stage, as altered by the servo loop. One is the integrator RC time constant, which sets the integrator stage's -3dB frequency point, $f_{(U2)}$ (not the overall system -3dB point). The integrator 3dB point is:

NON-INVERTING GAIN STAGE WITH DC SERVO

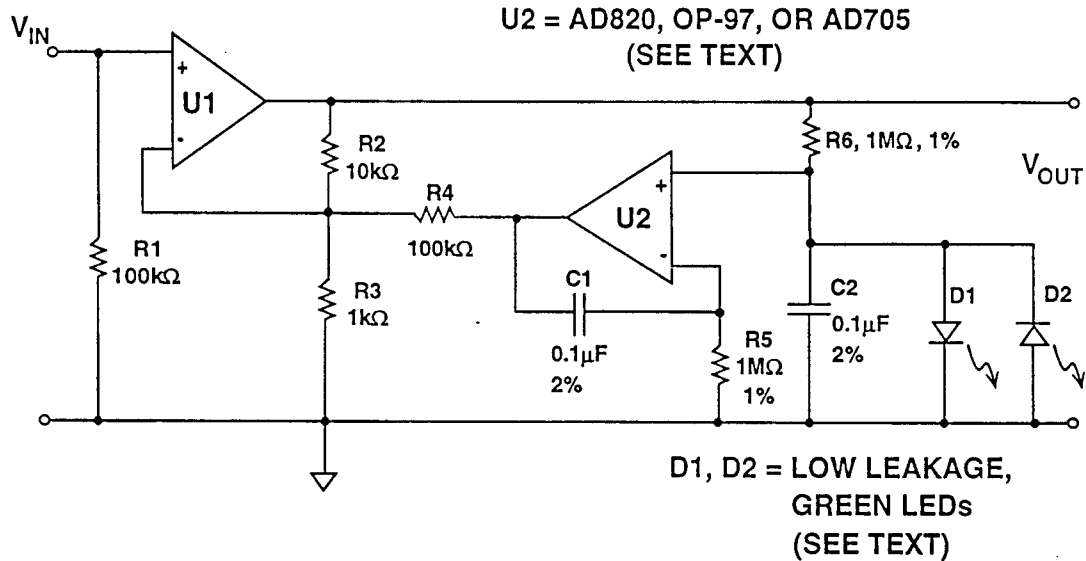


Figure 8.68

$$f_{(U2)} = \frac{1}{2\pi R_5 C_1} \quad \text{Eq. 8.24}$$

where $R_5 = R_6$, & $C_1 = C_2$.

A second factor is the total DC transfer ratio of the circuit, measured from the U2 input to the U1 output, or servo sense point. If this is defined "1/n", then a modified expression for the overall circuit's -3dB point can be written as:

$$f_{(3dB)} = \frac{1}{n 2\pi R_5 C_1} \quad \text{Eq. 8.25}$$

where $n = R_4/R_2$, thus:

$$\frac{1}{n} = \frac{R_2}{R_4} \quad \text{Eq. 8.26}$$

The servo RC values should be selected first for reasonable values. Then, feedback resistor R_4 is chosen several times higher than R_2 , making "n" large and "1/n" small. In the example, 1/n is 0.1,

so the the rolloff point is about 0.16 Hz. In general the rolloff frequency should be around 1% of the low frequency limit of the signal being processed.

At the U2 amplifier input, low-leakage (≤ 100 pA) clamp diodes should clamp C_2 , to prevent possible latch up. Suitable diodes are ordinary green LEDs with a light shield such as shrink tubing (to eliminate photocurrents), or C-B junctions of 2N5088/89 NPN transistors. Servo amplifier U2 should be a unity gain compensated, low offset voltage, low-input-bias-current op amp. This can be either a FET-input device or a bias current compensated super- β bipolar. Possible choices are the AD711 or the OP-41 (FETs); or an OP-97 or AD705 (bipolar).

Note that most FET input op amps will need the clamp diodes to prevent phase reversal. When working on a common rail design (i.e., both the servo amplifier and amplifier being servo'd operate from common rails), there are exceptions to this behavior. These are the AD820 and AD822 op amps, which, as single supply designs, have working input CM ranges which include the negative rail. As such they can be used without special precautions against latchup, and they also serve very well as integrators due to their very low bias current of 2pA and their rail-rail output swing. Given these characteristics, the AD820 and AD822 are especially suitable for the application.

Any servo amplifier IC working on supplies lower than that of the servo'd

amplifier must use the clamping diodes. An audio power amp, for example, may swing ± 50 V at its output, and such potentials can cause malfunction or outright destruction in lower voltage servo ICs.

U1, and its associated circuitry, can take on many forms more complex than the one in this basic example. U1 might be a high output swing power amplifier. The servo loop would still operate as described, and correct not only offset errors due to U1, *but also any varying DC input level to U1*. The servo technique can be useful for continuous correction of high bias current, high offset or high drift. (It will even stabilize thermionic valves— another exercise for the historically minded reader).

Ensure that the worst-case offset to be corrected at the input of U1 is within the dynamic range defined by the values assigned for R_2 - R_3 - R_4 , the specific supply voltages used for U1-U2, and the clamps. High-quality low-leakage 1 or 2% film capacitors should be used in the integrator along with 1%, 50ppm/ $^{\circ}$ C metal-film resistors. Since these components will be high-impedance, lead lengths should be minimized around U2, and the assembled circuit should be carefully cleaned of any flux residue. The outside foils of both C_1 and C_2 should be connected to the lower impedance of the two nodes.

INVERTING GAIN STAGE WITH SERVO

An inverting stage with servo offset correction is shown in Figure 8.69, and uses a familiar inverting integrator for feedback. In this circuit, U1 is an in-

verting audio stage with a gain of R_2/R_1 . DC feedback from the U2 integrator stage is applied to U1 through the divider, R_4 - R_3 .

INVERTING GAIN STAGE WITH DC SERVO

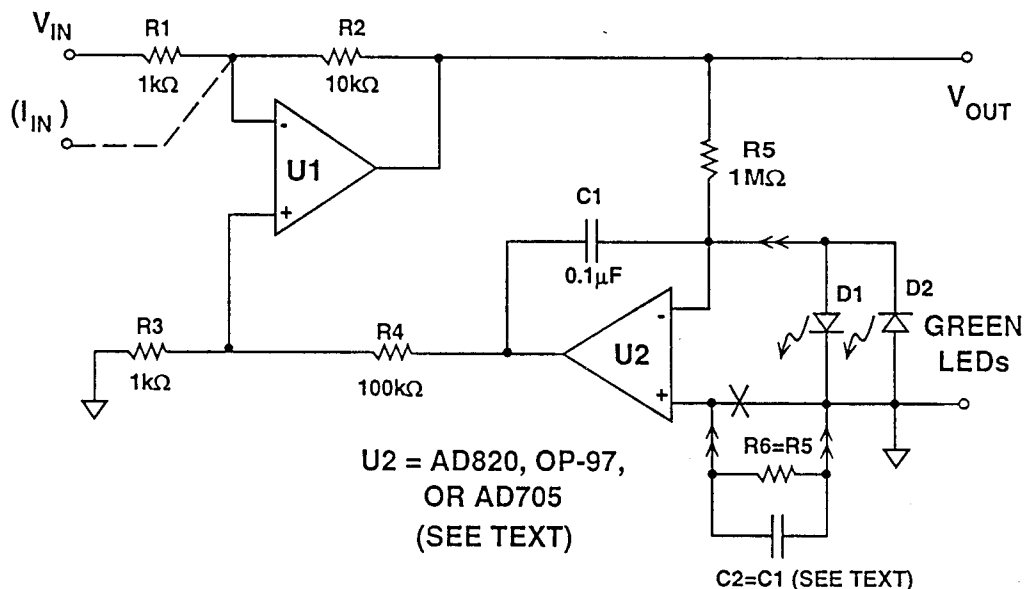


Figure 8.69

In this circuit the $1/n$ scaling factor around the U2-U1 DC loop is:

$$\frac{1}{n} = \left(\frac{R_3}{R_3 + R_4} \right) \left(\frac{R_1 + R_2}{R_1} \right) \quad \text{Eq. 8.27}$$

which is used to calculate the circuit's effective rolloff. With the time-constant values shown and the scaling of R_4 - R_3 , the circuit of Figure 8.69 has a low frequency cutoff of about 0.17 Hz.

When used just as shown with the U2 noninverting input grounded, clamping

diodes may not be necessary if they are integral to U2, as they are in the AD705 and OP-97. For higher bias current amplifiers at U2, the compensation network R_6 - C_2 may be used, in which case low-leakage input clamp diodes are recommended. In any case, the use of quality components for R_5

and C_1 is important. Again, R_4 should be about ten times R_2 (with R_1 and R_3 equal), and the supply voltage used for U1-U2 must be sufficient to accommodate the worst DC offset expected of U1. This circuit also works with more complex inverting stages, including discrete ones.

In principle, a *non inverting* integrator could also be used, with DC feedback to the R_1 - R_2 junction. The inverting integrator is more simple overall, however, and eliminates one RC network. This circuit works well when U1 has a current input.

From a system point of view, the "1/n" scaling factor of the servo can be very useful in extending the low frequency range of these two basic designs. A DC

attenuator or "tee" network can be placed between the U1 output and the integrator, and will work in a similar fashion for 1/n frequency scaling.

However, this particular frequency scaling approach should be used with caution, as it has the side effect of increasing the input offset of integrator U2 by the amount of attenuation. The output offset of U1 is then higher. For modest attenuations prior to the integrator (≤ 10 times), the circuit can be useful with the AD705 or OP-97 or similar devices, as their worst case offset is below $100\mu\text{V}$. In general, the offset multiplication effect prevents most amplifiers from being used with substantial (≥ 10 times) input attenuation prior to R_5 .

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